



JOINT STATEMENT OF THE 21st MEETING OF WORLD SEMICONDUCTOR COUNCIL (WSC)

MAY 18, 2017

Kyoto, Japan

The world's leading semiconductor industry associations – consisting of the Semiconductor Industry Associations in China, Europe, Japan, Korea Chinese Taipei and the United States – held the 21st meeting of the World Semiconductor Council (WSC) today. This meeting, held in Kyoto, Japan, was conducted under the “Agreement Establishing a New World Semiconductor Council,” approved at the third WSC meeting and signed on June 10, 1999, and amended on May 19, 2005.

The WSC meets annually to bring together industry leaders to address issues of global concern to the semiconductor industry. The WSC has the goal of promoting cooperative semiconductor industry activities, to expand international cooperation in the semiconductor sector in order to facilitate the healthy growth of the industry from a long-term global perspective. It also supports expanding the global market for information technology products and services. Further, it promotes fair competition, technological advancement, and sound environmental, health and safety practices. The WSC's mandate is also to encourage cooperation in such areas as environment, safety and health practices, protection of intellectual property rights, open trade, investment liberalization, and market development.

All WSC activities are guided by a dedication to fairness and market principles consistent with the World Trade Organization (WTO) rules and

the WSC member associations' bylaws. The WSC reaffirms that markets should be open and competitive. Antitrust counsel was present throughout the meeting.

The meeting was chaired by Mr. Tetsuya Tsurumaru, Chairman of Renesas Electronics Corporation and chair of the host delegation, Semiconductor Industry Association in Japan. Mr. Tsurumaru welcomed the delegates to Kyoto. The other delegations attending the 21st WSC meeting – Semiconductor Industry Associations in China, Europe, Korean, Chinese Taipei, Japan, and the US – were chaired, respectively, by Mr. Tzu-Yin Chiu of Semiconductor Manufacturing International Corporation, Mr. Klaus Meder of Robert Bosch GmbH, Mr. Seung Kook Synn of SK hynix, Mr. C.C. Wei of TSMC, and Mr. Tunç Doluca of Maxim Integrated Products.

During the meeting, the following reports were given and discussed, and related actions were approved:

Analysis of Semiconductor Market Data

The WSC reviewed a semiconductor market report covering market scale, market growth and other key industry trends. Per WSTS data, in 2016 the semiconductor market remained stable with a recorded value of US\$339 billion, slightly up from 2015. The Asia Pacific and China markets accounted for more than 60% of the global market, China still remains the largest region and on a growing trend. With respect to applications, the automotive and industrial end use sectors had the highest growth rates but the communications and computer segments remained the largest. Among the semiconductor product categories, sensors recorded an outstanding growth rate of 22.7%, followed by analog with a 5.8% growth rate and discretely with a 4.3% growth rate.

In addition to the market analysis, a special report focusing on Robotics and AI was presented to show their promising forecast market scale, as well as several semiconductor opportunities. The semiconductor industry may obtain approximately 10-20% of that revenue. Therefore, WSC should keep paying attention to the Robotics/AI market.

Cooperative Approaches in Protecting the Global Environment

The WSC is firmly committed to sound and positive environmental policies and practices. The members of the WSC are proactively working together to make further progress in this area.

(1) PFC (Perfluorocompound) Emissions

The global semiconductor industry is a very minor contributor to overall emissions of greenhouse gases, and the industry is continuously working to further reduce our contribution to emissions of GHGs. One important part of our GHG emission reduction efforts is our voluntary reduction of PFC gas emissions. In 1999, the WSC (consisting at that time of each of the original regional semiconductor associations in the U.S., the European Union, Japan, Korea, and Chinese Taipei) agreed to reduce PFC emissions by at least 10% below individual baselines for each regional semiconductor association by the end of 2010. The WSC has previously announced that the industry had far surpassed this goal. Over the 10-year period, the WSC has achieved a 32% reduction. In 2011, the WSC also announced a new voluntary PFC agreement for the next 10 years. The elements of the 2020 goal include the following:

- The implementation of best practices for new semiconductor fabs: The industry expects that the implementation of best practices will result in a Normalized Emission Rate (NER) in 2020 of 0.22 KgCO₂e/cm² equivalent to a 30% NER reduction from 2010 aggregated baseline. Best practices will be continuously reviewed and updated by the WSC.
- The addition of “Rest of World” fabs (fabs located outside the WSC regions that are operated by a company from a WSC association) in

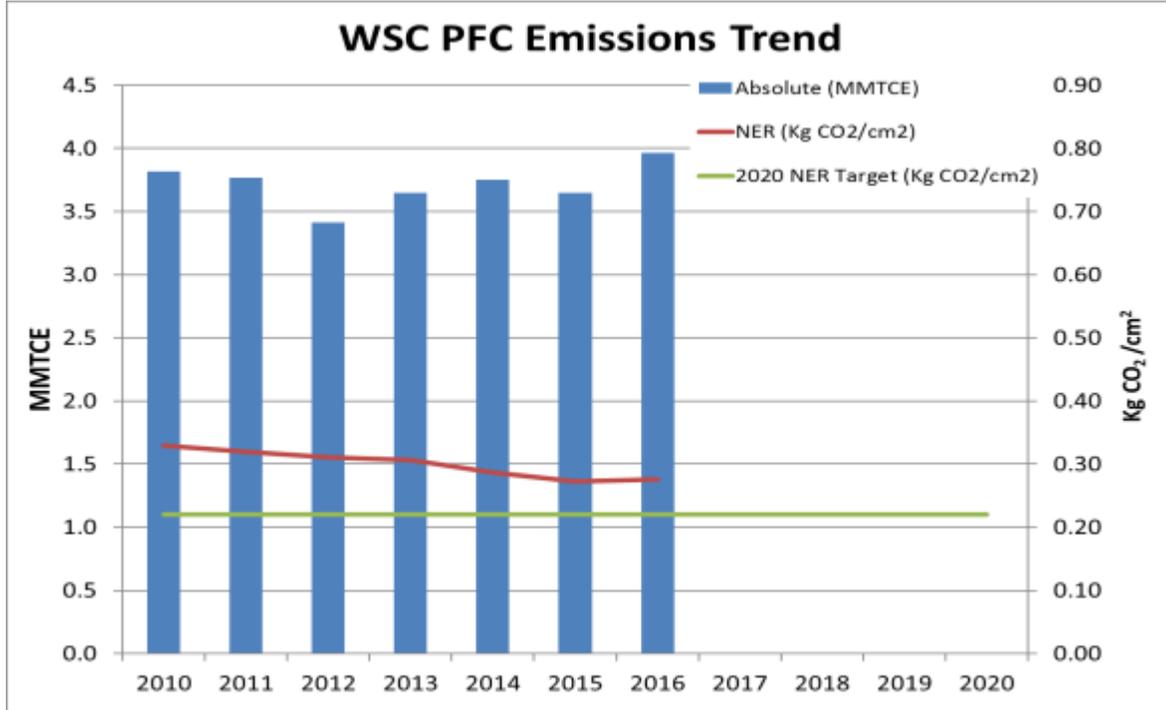
reporting of emissions and the implementation of best practices for new fabs.

- A NER based measurement in kilograms of carbon equivalents per area of silicon wafers processed ($\text{KgCO}_2\text{e}/\text{cm}^2$) that will be a single WSC goal at the global level.

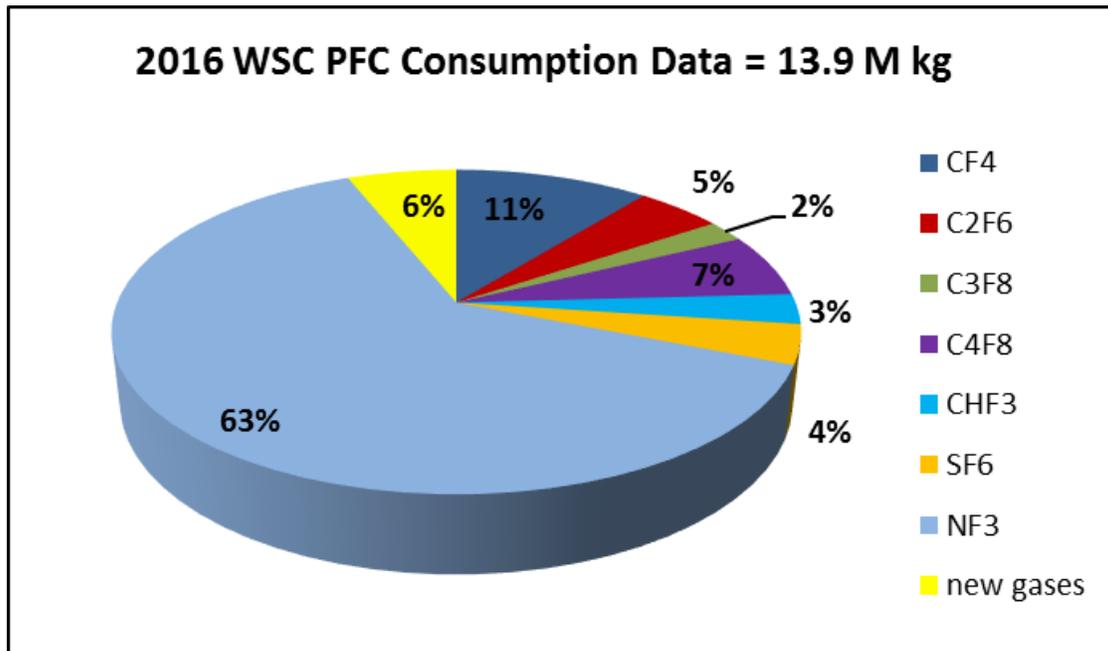
The WSC agreed to report its progress on this new voluntary agreement on an annual basis. This external reporting will provide aggregated results of the absolute PFC consumption and emissions alongside each other and NER trends. These figures represent combined emissions for the six WSC regional associations, in their own regions and in the “Rest of World” fabs described above. In addition, to improve transparency, the WSC has made its Best Practices for PFC Reduction document available previously on the WSC website. As part of this 2016-year data reporting the WSC has also revised its best practices document and will publish this update on the WSC website. The 2016 reporting also includes the reporting of newly used gases CH_2F_2 , C_4F_6 , C_5F_8 and $\text{C}_4\text{F}_8\text{O}$. In addition, the WSC reports the individual gas breakdowns.

The sixth-year results are as follows: in 2016, combined WSC absolute emissions of PFCs increased by 3.9% above 2010 to 3.97 MMTCE in 2016. The NER decreased by 16.1 % compared to 2010 to $0.28\text{Kg CO}_2/\text{cm}^2$. Please see the graph below which compares these results to $0.22\text{Kg}/\text{cm}^2$ equivalent to a 30% NER reduction anticipated by 2020.

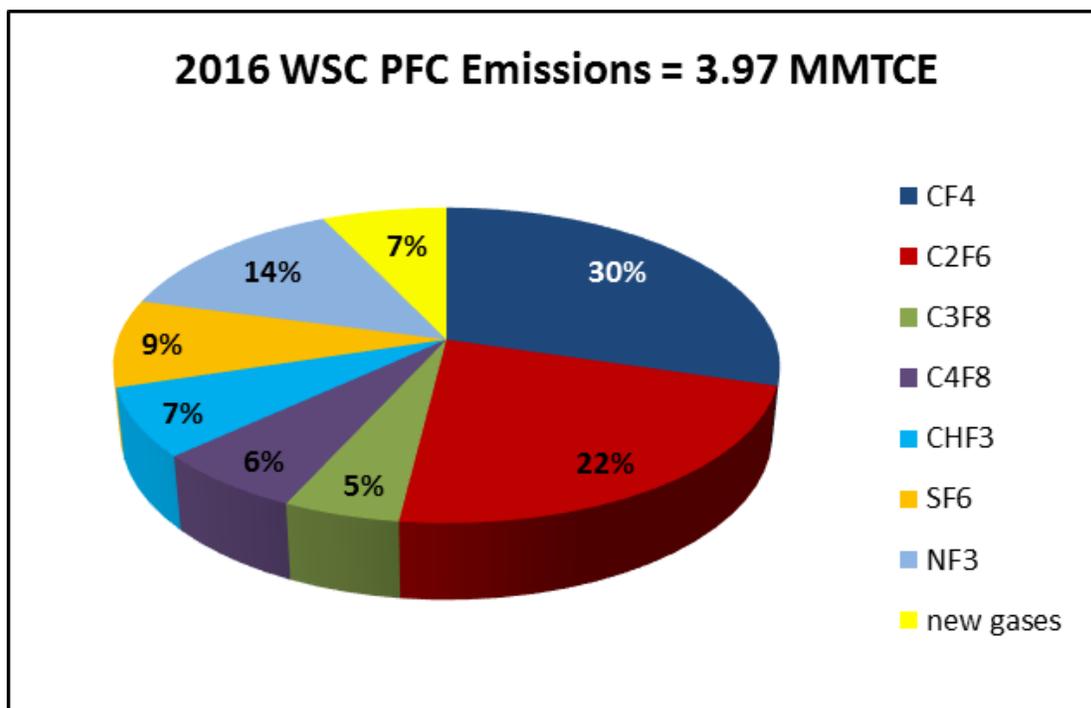
Results of WSC PFC Emission Trends



2016 WSC PFC Consumption and Emissions Data



(New gases include CH₂F₂, C₄F₆, C₅F₈ and C₄F₈O)



In order to ensure the continued accuracy of WSC reporting on PFC emissions, the WSC calls on the GAMS to work with the Intergovernmental Panel on Climate Change (IPCC) and industry experts to update the guidelines applicable to reporting of emissions from semiconductor fabs to reflect the most current and best available data.

(2) Chemical Management

The WSC is pleased to announce today that the companies participating in the WSC have successfully eliminated the remaining critical uses of (perfluorooctyl sulfonate) (PFOS) in semiconductor manufacturing processes. This elimination is a major environmental management achievement for the worldwide semiconductor industry that has been working on managing and substituting PFOS. Further details of this achievement can be found in Annex 1 of this May 18th 2017 WSC Joint Statement.

The WSC recommends that Governments/Authorities inform their appropriate environmental regulatory ministries and the UN Stockholm Convention of this successful action by the global semiconductor industry.

The WSC is aware that governments around the world are considering taking action on other chemicals of interest to the semiconductor industry, despite our industry's success in phasing out PFOS. **The WSC reiterates its recommendation that Governments/Authorities proceed carefully in regulating chemicals that are essential to the semiconductor industry.**

The WSC recommends that Governments/Authorities take into account the limited potential risk of exposure from uses in the semiconductor industry and our supply chain, the management practices in the semiconductor industry, the small quantity of chemicals used in manufacturing processes or contained in articles, and the fact that these chemicals are not intended to be released from the finished product under normal conditions of use.

The WSC further recommends that any regulations provide the semiconductor industry with sufficient time to evaluate our uses of chemicals that may be subject to potential regulation and the uses within our supply chain. If restrictions on chemicals used in our industry are deemed to be necessary and appropriate for the protection of human health and the environment, the WSC recommends that Governments/Authorities provide sufficient time for the industry to identify, qualify, and transition to alternative chemicals that satisfy our functional and performance requirements, and be provided with exemptions to allow continuation of critical uses of these chemicals in processes and articles. In addition, where regulations cover articles, the threshold levels in regulations should be harmonized globally and be technically feasible.

(3) Resource Conservation

Semiconductor devices contribute to improved resource conservation in our world. Energy efficiency enabling semiconductors play a key role in the more efficient transmission, distribution and consumption of

energy which also largely contributes to world's carbon emission reduction, contributing to humankind's achieving the United Nation's carbon reduction goal under the global climate change risk mitigation.

Traditional forms of energy and renewable energy sources will not be sufficient alone to meet the world's future energy needs. Consuming energy more efficiently is therefore of paramount importance, and semiconductor devices help achieve this goal. Semiconductor devices enable a more efficient use of energy in all aspects of our daily lives: in the home, office or on the road; in industrial manufacturing; in public infrastructure; and in public transport. The semiconductor sector itself is not a large natural resource consumer amongst global industries. However, the WSC's members continue to focus activity on reducing the use of resources involved in the device manufacturing processes to reduce the direct impacts to the local and global environment. The semiconductor sector will continue to pursue environmental conservation programs in its fabs in the areas of energy, water and waste and the industry will continue to share examples of improvement practices.

Conflict Minerals

The WSC adopted at its 17th meeting in May 2013 a Conflict-Free Supply Chain Policy in order to support the global progress in addressing the sourcing of conflict minerals from conflict zones, such as the Democratic Republic of the Congo (DRC) and surrounding countries.¹

The global semiconductor industry is a recognized leader in addressing conflict minerals. The semiconductor industry has led the development of compliance tools (such as the OECD due diligence guidance framework) that have been readily adopted by other key industry sectors and has implemented state of the art programs to track progress across our

¹ "surrounding countries" as defined under the Dodd-Frank Wall Street Reform Act 2012 (Central Africa Republic, South Sudan, Zambia, Angola, The Republic of the Congo, Tanzania, Burundi, Rwanda, Uganda)

entire supply chain.

The WSC continues to make progress towards a Conflict-Free Supply Chain Policy. The WSC has undertaken industry surveys with its members to ascertain the state of progress of implementation of this conflict free supply chain policy across the industry for years 2014, 2015 and 2016. These surveys indicate that although the industry as a whole is not currently conflict free, significant progress and improvements have been made over recent years. Surveys identify also that more semiconductor customers are reviewing conflict minerals programs of the industry and many semiconductor companies have been required to become conflict mineral free or have been requested for a third party certification. The surveys also highlight that most of the industry see reaching out to smelters/refiners to become compliant (certified) and phasing out non-compliant smelters/refiners in the supply chain as some of the biggest challenges. The EICC-GeSI² conflict minerals reporting template (CMRT) or a similar format for supplier data gathering is still the most commonly used reporting tool by the industry.

The WSC continues to promote the use of industry-standard tools, control-points, methods and standards among WSC member associations to facilitate continued industry progress towards a conflict free supply chain policy. The WSC also welcomes the certification of more global smelters and refiners through the Conflict-Free Smelter Program (CFSP) as a positive development.

The WSC would recommend that if GAMS members are considering new conflict minerals type legislation, that the legislation should be globally aligned to ensure that such legislations promote the

² Electronic Industry Citizenship Coalition (EICC) and Global e-Sustainability Initiative (GeSI)

harmonization of global efforts in creating a conflict-free supply chain and should utilize existing industry-wide compliance tools (such as the OECD due diligence guidance framework) and initiatives (such as Conflict Free Sourcing Initiative) and be based on voluntary principles. The WSC welcomes the approach taken by the EU authorities in finalizing their conflict minerals related legislation in 2017.

Effective Protection of Intellectual Property

(1) Abusive Patent Litigation (NPEs/PAEs)

WSC recognizes that abusive patent litigation seriously undermines innovation by redirecting research expenditures and other resources to unnecessary litigation expenses, and by making it more difficult to bring products to market. The WSC supports the continued focus on preventing abusive patent litigation.

In view of this, the WSC supports a range of “best practices” in regard to the issue of abusive patent litigation, including NPEs/PAEs, and, as a result, has developed and adopted a set of “Abusive Patent Litigation (Including NPEs/PAEs): Best Practices to Combat Abusive Patent Litigation,” as set forth in Annex 2 to this Joint Statement.

The WSC calls on governments and authorities to support these Best Practices in addressing abusive patent litigation practices.

(2) Trade Secrets

The WSC supports national legislative initiatives to improve the protection of trade secrets. The WSC reminds government and authorities to support and implement “Core Elements for Trade Secret Protection Legislation” in Annex 1 to the 2015 WSC Joint Statement, when making the

national trade secret protection legislation, and any related pending legislation or legislative reforms or amendments.

The WSC will continue with discussions on this topic.

(3) Patent Quality

The WSC continues to collaborate with the World Intellectual Property Organization (WIPO) with respect to improving Patent Quality. In particular, WIPO has invited WSC's support on the patent quality aspects of WIPO's annual survey to member patent offices.

The WSC encourages GAMS to support WSC's continuing initiatives with WIPO on improvement of patent quality.

Fighting the Proliferation of Semiconductor Counterfeiting

As noted in past WSC statements, the proliferation of counterfeit semiconductor products creates serious risks to public safety and health and to critical infrastructure.

The WSC commits to intensify anti-counterfeiting work activities through its Anti-Counterfeiting Task Force. This Task Force has circulated widely the WSC's White Paper "Winning the Battle against Counterfeit Semiconductor Products" that describes the risks from counterfeit products. The WSC's White Paper will be updated once new data and information are available. Anti-Counterfeiting Task Force has distributed a semiconductor anti-counterfeiting poster for awareness raising at exhibitions and seminars; and has shared examples of anti-counterfeiting capacity building measures that could be employed across the semiconductor industry. The WSC Anti-Counterfeiting Task Force continues with these efforts.

The WSC supports for the Global Anti-Counterfeiting Group's (GACG) World Anti-Counterfeiting Day on June 7, 2017 to increase awareness of the public health, safety and other performance risks caused by counterfeits. Please refer to Annex 3.

The WSC appreciates the GAMS' reconfirmation, at its 2016 meeting, to the GAMS' commitment to fighting semiconductor counterfeiting and to work with their customs and law enforcement authorities to intensify the implementation of semiconductor anti-counterfeiting enforcement measures, including information-sharing activities.

The WSC calls on GAMS members to continue to implement appropriate measures (including domestic, bilateral and multilateral countermeasures) to deal with counterfeit semiconductors.

The WSC supports GAMS members in employing proactive enforcement measures, including strict search and seizure, and working closely with the industry and also welcomes GAMS coordination with their customs and law enforcement authorities.

The WSC looks forward to continued coordination with GAMS in stopping counterfeits at the borders and vigorously prosecuting perpetrators who make and distribute counterfeits, and will continue to cooperate with GAMS customs and enforcement authorities in these efforts.

Encryption Certification & Licensing Regulations

The WSC commends the GAMS commitment to observe the WSC Encryption Principles and recommendations, and to encourage other governments to take the WSC Encryption Principles into account when formulating policies and regulations in order to avoid a negative impact on the industry competitiveness and prevent unnecessary restrictions to trade. The WSC notes that the 2016 GAMS Chairs summary emphasized:

- Importance of meaningful stakeholder participation whenever regulations, procedures, or requirements on the importation or use of commercial encryption are created or revised
- The need for continuous review of new measures
- The need for enhanced WTO notification and to fully respect relevant WTO obligations.

The WSC Encryption Principles underscore free market access, transparency and non-discrimination for commercial encryption products, the adoption of international standards, and open procedures and rules, in line with WTO notification rules. The WSC emphasizes that the WSC encryption principles should apply to all commercial applications, including most critical information infrastructure (CII) applications. Allowing the use of commercial cryptography in connected products used in CII enables cost-effective support for business continuity, including interoperability and compatibility with other systems.

The WSC appreciates GAMS' acknowledgment of the need to review the global regulatory environment on encryption, especially as encryption technologies play an increasingly critical role in securing commercial products and applications. The WSC has examined regulatory initiatives on cybersecurity in GAMS and non-GAMS countries and regions. It has found that different regulatory approaches exist in both GAMS and non-GAMS regions, some of which are discriminatory and impose unnecessary restrictions to trade, and, as such, are inconsistent with WSC encryption principles.

The WSC believes protecting CII is about ensuring the continuity of important infrastructures and economic activities whereas national security should be treated separately. **The WSC strongly encourages GAMS members, at the next GAMS, to share information as to how WSC Encryption Principles apply to all commercial applications, including, but**

not limited to, most CII applications and discuss new developments related to encryption.

The WSC reiterates the need for global convergence in applying different international standards and certification procedures, and for collaborative international approaches when developing and implementing cryptographic solutions, including public availability of algorithms. Such an approach inherently promotes more secure products, and allows innovation and the digital economy to flourish.

Customs and Tariffs

(1) Information Technology Agreement (ITA) and ITA Expansion

The WSC welcomed the successful conclusion of the expansion of the ITA as it ensures tariff-free treatment for a wide range of semiconductor products, including advanced devices such as Multi-component Integrated Circuits (MCO) as well as for Multi-chip Integrated Circuit (MCP). The WSC vigorously supported the ITA expansion negotiations and the inclusion of these products in the ITA. The WSC is grateful to GAMS for the pivotal role it played both in the 2006 “Agreement on Duty Free Treatment of MCP,” and in achieving the 2012 consensus definition for MCO, which as such was included in the expanded ITA and the 2017 review of the harmonized system of customs tariffs.

According to WSC members’ information, a number of MCO products, which up until January 1, 2017 were duty-free when imported into one region, are currently facing import duties for the first time. This is contrary to the purpose and spirit of the ITA expansion which seeks to eliminate tariffs in order to contribute significantly to the dissemination of information technology and the expansion of global value chains. **The WSC**

requests that the GAMS work to immediately ensure that no region imposes tariffs on MCO products which were previously tariff free.

WSC also calls on Parties considering to autonomously eliminate tariffs on semiconductor products earlier than foreseen in the staging schedule.

To maximize the benefits of the ITA expansion, the WSC also calls on GAMS to encourage additional WTO members to join the Agreement.

Broader membership in ITA expansion will more quickly lift the burden of tariffs on global economic growth and intensify the benefits of the ITA for all members. WSC members plan to participate in the WTO 20th Anniversary of the ITA Symposium in Geneva to highlight the substantial and long-term economic benefits offered by ITA expansion.

(2) Review of the ITA expansion product scope

The ITA expansion Parties unanimously agreed, in the Annex to the Ministerial Declaration on the Expansion of Trade in Information Technology Products of 16 December 2015, to meet no later than January 2018, to review the ITA expansion product coverage and consider whether, also in the light of technological developments it should be updated to incorporate additional products.

The WSC strongly supports the continuous update of the ITA product scope, to include new and evolving semiconductor technologies, to minimize administrative burden and ensure barrier-free international movements of goods, both of which are crucial for semiconductor manufacturing and innovation. **To this end the WSC encourage GAMS to work cooperatively with their services to ensure that ITA expansion parties meet no later than January 2018 to review the ITA expansion product coverage.**

In response to a request by GAMS in 2016 to provide information regarding technology advances for the purposes of updating the ITA, the WSC is compiling a non-exhaustive list of semiconductor industry products, manufacturing materials and equipment which are currently not covered by the ITA and ITA expansion. All associations will contact their respective GAMS members to discuss this list for potential inclusion in ITA. An inclusion of these items in an updated ITA would ensure free trade of innovative essential components and further bolster innovation, critical to the prosperity not only of the semiconductor industry but of international economies.

The WSC requests GAMS members to work cooperatively to ensure that the above-mentioned list will be considered during the meeting of ITA expansion parties where the ITA expansion scope will be discussed.

(3) Semiconductor based transducers

WSC welcomes the GAMS' endorsement for the definition of semiconductor-based transducers proposed by the WSC in 2016, and the GAMS' support for advancing WCO work on the definition, for the purpose of amending Heading HS 8541 in the HS 2022 revision. Semiconductor-based transducers are for the purpose of this definition semiconductor-based sensors, semiconductor-based actuators, semiconductor-based resonators and semiconductor-based oscillators.

WSC also applauds the initiative by the European Commission to submit to WCO a revised semiconductor-based transducer proposal based on the WSC and GAMS consensus for discussion in the 52nd Session of the WCO HS Review-Subcommittee in May 2017.

WSC calls on GAMS to continue to support this proposal and cooperate with its Customs agencies to achieve the implementation of this amendment to heading 8541 within the HS2022 review.

(4) Customs Classification for Semiconductors

The WSC remains committed to working with GAMS Customs agencies and the World Customs Organization (WCO) to achieve optimal and uniform Customs classification for semiconductors.

In 2015 and in 2016 the WSC provided WCO with detailed cases of identical semiconductor products classified differently in different countries, and recommended that the products identified be treated as semiconductor products, namely classified under HS heading 8541 or 8542 as guided by Note 9 in Chapter 85 of the Harmonized System which gives these headings precedence in the classification of these articles.

On 16th of March 2017, WSC delegates met with representatives of Customs agencies from five of the six GAMS member regions to discuss challenges in semiconductor HS classification. The WSC delegates explained that the gap between rapid innovation in semiconductor technology and the multi-year HS nomenclature international alignment processes has resulted in HS definitions that are complex and difficult to administer or do not cover new innovative semiconductor products. This leads to higher likelihood of differing interpretations, which results in classification inconsistencies or in semiconductor products being classified outside of the semiconductor headings 8541 and 8542. Divergent classifications and complex product descriptions cause an increased administrative burden both for Authorities and semiconductor companies, are more likely to give rise to disputes, and make free trade agreements more complex to achieve. In the meeting, WSC called on Customs agencies to work cooperatively to solve these issues. During the discussion, Customs delegates suggested that if a more generic, but still comprehensive definition of semiconductors would be in place, classification challenges could be eased. Customs agencies indicated that the WSC could consider discussing and developing such suggested generic definition.

The WSC is thankful to Customs agencies for their constructive cooperation with the WSC and for their guidance. The WSC endeavours to work on a generic and simpler definition proposal of semiconductors, and

to share it with Customs agencies and GAMS when and as appropriate. **WSC calls on GAMS to support this work and encourages their Customs agencies to cooperate with WSC.**

Further, WSC is working with Customs agencies and the WCO to include semiconductor based transducers under heading 8541 and a modified definition of MCP products (clarifying that also products in which not all ICs are electrically interconnected will be considered as MCP as per Annex 3) within the HS2022 review. **WSC calls on GAMS to support these proposals and encourages their Customs agencies to cooperate with WSC.**

(5) AEO/Trusted Traders

Semiconductor companies continue to invest substantially to comply with trusted traders' policies, such as the Authorized Economic Operators' (AEO) programs, which are in place in countries worldwide. These policies aim at improving cargo and supply-chain security to reduce the number of cases where threat to security is expected. Most semiconductor companies have achieved AEO status, many of them in multiple jurisdictions worldwide.

To further facilitate the import-export operations for trusted traders, the WSC believes it is crucial to establish a core set of internationally accepted and tangible trade facilitation benefits to be provided to AEOs under all relevant national programs. Such benefits should be transparent, meaningful and should justify the additional costs sustained by economic operators in meeting the requirements prescribed by the trusted traders' programs.

In 2016, the WSC had shared with GAMS key examples of proposed trade facilitation benefits and measures, and it has continued working to detail these examples. The WSC would like to share with GAMS the current status of its work. Annex 5 includes concrete and detailed recommendations for trade facilitation measures. **The WSC calls on GAMS to consider these recommendations, discuss them with their Customs**

agencies and explore ways to achieve a common understanding of how these recommendations could be implemented and practically applied in AEO programs.

In order to facilitate the above, WSC recommends that GAMS support the organization of a workshop or seminar on AEO/Trusted Traders be conducted with Customs agencies from GAMS regions. Purpose is to develop a dialogue with customs in order to realize more tangible benefits for semiconductor industry. Such workshop could be organized in proximity to relevant internationally recognized Customs agency events. WSC asks GAMS to support this proposal and encourage their Customs agencies for active participation.

Regional Support Programs & Regional Stimulus

WSC reiterates its view that government actions and assistance in the semiconductor sector should be transparent, open and avoid adoption of protectionist, discriminatory or trade-distorting measures.

Per GAMS' request at the 2016 Berlin Meeting for WSC recommendations on how to implement these principles in practice, the WSC proposes the "GAMS Regional Support Guidelines and Best Practices." WSC requests GAMS to consider adopting Best Practices for Regional Support aligned with the WSC recommendations for guidelines and best practices at its 2017 GAMS meeting.

The WSC welcomes the GAMS' decision to further study and exchange information on relevant regional support programs at a 2nd Workshop at the 2017 GAMS meeting. The WSC hereby presents to GAMS its proposed workshop agenda. The WSC requests that GAMS members identify appropriate officials or individuals responsible for or familiar with

government support programs in their region to participate in this workshop.

Growth Initiatives

WSC supports policies that unleash the enormous potential for economic and societal benefits from semiconductor technology including enhanced automotive safety, innovative medical applications, energy efficiency and intelligent systems. Spreading the benefits from semiconductor technology can only be achieved through deep and lasting partnerships across industries and between industry, government and academia. All stakeholders must work together on R&D to solve fundamental challenges, ensure interoperability, promote security of connected systems, and establish sound public policies.

The WSC is committed to initiatives aimed at accelerating the rate that semiconductor technologies are adopted in emerging sectors, including sharing published research, engaging in dialogue with other industry sectors and regulators, issuing reports on emerging application markets, and advocating for public policies and agreements that promote growth, such as the Environmental Goods Agreement (EGA).

In addition to the policy recommendations included elsewhere in this Joint Statement, the WSC encourages governments and authorities to help enable new and innovative semiconductor technology applications by:

- 1. Supporting basic and pre-competitive R&D to overcome technical challenges, especially in the areas of low-power computing, energy efficient sensing, security of connected systems, storage, and wireless connectivity.**

2. **Promoting interoperability by adopting technology-neutral policies, and working together to create common standards/policies for wireless connectivity, storage, data security, encryption, etc.**
3. **Working with industries so that regulations in fields such as automotive and health care encourage investment in and adoption of new digital processes/technologies in industries.**
4. **Supporting policies that open markets and streamline trans-border data flow, including eliminating tariffs on environmental goods.**
5. **Working to restart and swiftly conclude the WTO Environmental Goods Agreement.**

The WSC notes the important role the WTO plays in creating new opportunities for trade that directly benefit semiconductor consumers. There is a substantial opportunity at the 11th WTO Ministerial to be held in Buenos Aires in December 2017 to add impetus to the WTO's e-commerce and digital trade agenda and obtain specific progress on issues of vital interest to our industry and our respective economies. Such opportunities include increasing ITA participation and product coverage, and promoting environmental goods. **We urge GAMS to agree at its October 2017 meeting to cooperate on enhanced efforts within the WTO to support a strong and positive WTO agenda on e-commerce at the Buenos Aires WTO Ministerial in order to create new opportunities for semiconductor growth and trade.**

The WSC notes in particular that, as highlighted above in the WSC's market report, accelerating trends in artificial intelligence ("AI") and robotics reflect new technologies that point to significant and positive economic and social impacts in the years ahead. Together, machine

learning, natural-language recognition, biometrics, and decision management are converging toward what the World Economic Forum has described as the Fourth Industrial Revolution. Semiconductors are a driving force in this AI revolution. The WSC is committed to developing innovative technologies and promoting policies that will advance these significant developments, and the WSC intends to focus further efforts on this subject.

Approval of Joint Statement and Approval of Recommendations to GAMS

The results of today's meeting will be submitted by representatives of WSC members to their respective governments/authorities for consideration at the annual meeting of WSC representatives with the Governments/Authorities Meeting on Semiconductors (GAMS) to be held in October 2017 in Busan, Korea.

Next Meeting

The next meeting of the WSC will be hosted by the Semiconductor Industry Association in US, and will take place in San Diego, California May 2018.

Key Documents and WSC Website:

All key documents related to the WSC can be found on the WSC website, located at:

<http://www.semiconductorcouncil.org>

Information on WSC member associations can be found on the following websites:

Semiconductor Industry Association in China:

<http://www.csia.net.cn>

Semiconductor Industry Association in Europe:

<http://www.eusemiconductors.eu>

Semiconductor Industry Association in Japan:

<http://semicon.jeita.or.jp/en/>

Semiconductor Industry Association in Korea:

<http://www.ksia.or.kr>

Semiconductor Industry Association in Chinese Taipei:

<http://www.tsia.org.tw>

Semiconductor Industry Association in the US:

<http://www.semiconductors.org>

Annexes:

1. WSC Announces Successful Completion of PFOS Elimination Agreement
2. Abusive Patent Litigation (Including NPEs/PAEs): Best Practices to Combat Abusive Patent Litigation
3. 2017 World Anti-Counterfeiting Day – WSC Press Release
4. Proposal for the amendments of legal notes to HS Chapter 85 for Multichip-ICs and for the corresponding HS explanatory notes
5. Illustrative Examples of Enhanced Benefits for Trusted Traders

WSC Announces Successful Completion of PFOS Elimination Agreement

The WSC is pleased to announce today that the companies participating in the WSC have successfully eliminated the remaining critical uses of perfluorooctyl sulfonate (PFOS) in semiconductor manufacturing processes. This elimination is a major environmental management achievement for the worldwide semiconductor industry that has been working on managing and substituting PFOS. When scientists identified, environmental problems associated with PFOS and the regulatory authorities took steps to address the use of this chemical, the global semiconductor industry, even though it was only a minor user of the substance, proactively took steps to address its uses of the material.

In 2006, as part of the WSC's approach to sound Environment, Safety and Health (ESH) practices, the WSC and the semiconductor manufacturing industry supplier association (SEMI) announced publicly an agreement committing to end non-critical uses of PFOS chemicals in semiconductor manufacturing and to work to identify substitutes for PFOS in all critical uses for which no other materials were available at that time. The agreement also committed members of the WSC to collect and make available aggregated industry information to provide a transparent communication of industry progress. This was done through the WSC Joint Statement. Since this time, the WSC companies have expended significant resources to further understand and limit their PFOS uses, control and manage related emissions through high temperature incineration of PFOS containing solvent waste, evaluate potential wastewater discharge control technologies, and conduct research and development to identify alternatives and reduce and replace uses.

In 2011, the WSC announced as part of its regular reporting on the industry's progress on the PFOS agreement that it has successfully eliminated non-critical uses of PFOS in its manufacturing operations, and identified substitutes for most other uses. The remaining uses of PFOS at that time were limited and highly controlled, and emissions of PFOS by the semiconductor industry had been reduced by 99% from 2005 levels to approximately 6 kg/year in 2011. Since that time, the industry has continued its work phasing-out the remaining critical uses of this chemical. The WSC announces today that

the companies participating in the WSC have successfully eliminated the remaining uses of PFOS in semiconductor manufacturing.³

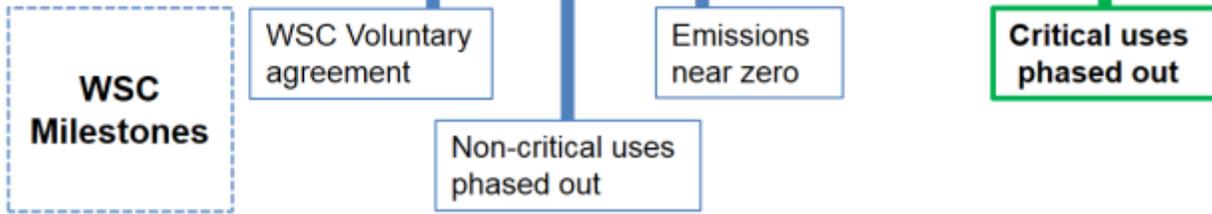
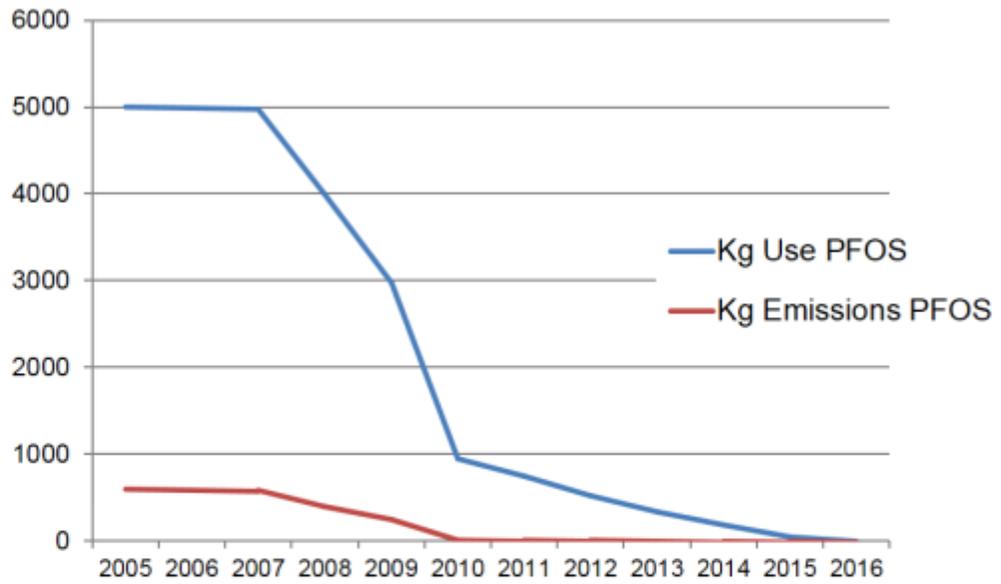
The semiconductor industry relies on chemicals that possess unique chemical and physical properties in the manufacture of advanced semiconductors. In order to etch billions of transistors on a piece of silicon the size of a centimeter, the industry employs highly sophisticated manufacturing equipment and key materials. In the past, the semiconductor industry used very small amounts of PFOS as critical ingredients in leading edge photoresists and antireflective coatings, materials used in the photolithographic process for imprinting circuitry on silicon wafers. The industry previously used PFOS because of its stability, integration with manufacturing tools, and unique functionality. The semiconductor industry's use of this chemical was small in comparison with several other industries.

The elimination of PFOS represents a major achievement of the WSC and the semiconductor manufacturing industry. This effort was the result of years of work by all companies in identifying appropriate substitutes and significant investments in development, process qualification, and process modifications.

The WSC recommends that Governments/Authorities inform their appropriate environmental regulatory ministries and the UN Stockholm Convention of this successful action by the global semiconductor industry.

³ Some WSC members and individual companies within the WSC have successfully completed the phase-out of PFOS in previous years, while other companies have more recently completed the phase-out. The WSC recognizes that some semiconductor companies outside of their membership may still use PFOS.

Global Semiconductor PFOS Elimination



Abusive Patent Litigation (Including NPEs/PAEs): Best Practices to Combat Abusive Patent Litigation

Over the last ten years, governments and authorities in various WSC member countries and regions have devoted, and continue to devote, significant focus and effort to the study of the impact of abusive litigation practices, including the impact of non-practicing patent entities (NPEs) and patent assertion entities (PAEs) on the economies and national legal systems of their jurisdictions.

The WSC, for its part, adopted in 2014 a series of specific recommendations addressing this issue, encouraging governments and authorities to adopt appropriate and balanced policies and legislative measures to regulate abusive litigation by patent holders, in order to help advance innovation and improve overall patent systems. In recent years, various governments/authorities have issued official statements of policy; proposed legislation; conducted economic studies; and enacted legislation directed at the economic and legal impact of such entities. The approach of different countries and regions, however, has varied, and not all countries and regions have fully implemented the WSC's recommendations.

Given this uncertain state of development and the continued harmful impact of abusive patent litigation practices (including NPEs/PAEs) on the semiconductor manufacturing industry, it is in the WSC's interest to share "best practices" in dealing with this issue. In its 2016 Chairman's Summary, the GAMS invited the WSC to undertake such an effort:

GAMS . . . invites WSC to share best practices on this issue {continuing problems caused by abusive patent litigation (including NPEs/PAEs)} and to report on these at the next GAMS meeting.

(Government/Authorities Meeting on Semiconductors, Chairman's Summary, Berlin, Germany, Oct. 20, 2016)

In response to the GAMS' invitation to share "best practices" on this issue, the WSC recommends the following best practices to reduce the potential for harm from abusive patent litigation conduct (including by NPEs/PAEs):

1. Timing of Damages and/or Permanent Injunction: Practices to ensure that damages and/or permanent injunction is not granted before both infringement and invalidity proceedings on a patent are concluded. Avoids abusive patent practices of trying to collect damages or having permanent injunctions granted on an invalid patent.

2. Standard for Injunctions: Injunctions should not be granted unless the plaintiff can show that it will suffer irreparable injury, the remedies available at law are inadequate to compensate for that injury, the balance of hardship between the parties favors the grant of an injunction, and the public interest would not be disserved.

3. “Forum Shopping”: Practices that prevent abuses in which plaintiffs “forum shop” to select “patentee-friendly” courts in which the plaintiff is more likely to ultimately prevail or at least obtain a preliminary injunction. Such initiatives may include, where practicable and effective, establishing courts with specialized patent expertise or addressing inequalities in venue selection that lead to abusive “forum shopping.”

4. Fee Shifting with Bonds: Practices that, in addition to encouraging fee shifting, require up front bonds or alternatively provide for other sufficient evidence to ensure the plaintiff could pay fee shifting costs should they apply. Otherwise, abusive patent litigators underfund themselves and simply declare bankruptcy if hit with paying the other side’s fees.

5. Means to Challenge Patent Validity: Practices that provide a fair, speedy, and cost-efficient means to challenge patent validity, such as the use of *inter partes* review (IPR) or other post-grant review procedures.

6. Publication of Pleadings and Opinions: Practices that require publication of non-confidential copies of pleadings and opinions, with a process for redacting any sensitive and/or confidential information belonging to the parties.

7. Defense Collaboration: Practices that encourage lawfully permissible collaboration among defendants being sued by the same plaintiff under the same patent, e.g., under a joint defense agreement, to ensure that the best defense possible is developed.

8. Real Parties in Interest: Practices that require the disclosure of the appropriately defined real parties-in-interest in litigation (see, e.g., WSC 2014 Joint Statement recommendation for greater patent ownership transparency in lawsuits).

9. Discovery Burden and Cost Asymmetries: Practices that encourage case management procedures to address discovery burden and cost asymmetries in NPE/PAE litigation (see, e.g., WSC 2014 Joint Statement recommendation to implement appropriate revisions and limits to discovery procedures).

10. Sufficiency of Pleadings: Practices that provide procedures to challenge the “plausibility” of pleadings in patent cases and to ensure that patent infringement complaints provide sufficient notice to accused infringers (see, e.g., WSC 2014 Joint Statement recommendation for heightened pleading requirements for patent lawsuits).

The WSC appreciates the invitation of the GAMS to identify the above best practices on the issue of abusive patent litigation (including NPEs/PAEs) and welcomes the opportunity for further discussion with GAMS on the most effective means to implement these best practices.



7 June 2017

FOR IMMEDIATE RELEASE

WSC supports World Anti-Counterfeiting Day

On Wednesday, 7 June 2017, the Global Anti-Counterfeiting Group (GACG) Network is celebrating the 19th edition of the World Anti-Counterfeiting Day (WACD). The World Semiconductor Council (WSC) strongly supports the WACD and believes it is a great initiative to highlight the anti-counterfeit measures being taken across industries. The World Anti-Counterfeiting Day enables the organisation of targeted events focusing on particular problems of counterfeiting & piracy under the umbrella of an international outreach campaign. This year's Global Anti-Counterfeiting Awards ceremony will also be held in Paris, France on WACD, 7 June 2017.

According to the Organisation for Economic Co-operation and Development (OECD), international trade in counterfeit goods represented up to 2.5% of world trade, or up to USD 461 billion⁴. In view of these staggering numbers, the WSC is convinced by the importance of an initiative such as the World Anti-Counterfeiting Day, and believes it to be a great way of highlighting the common cause of fighting counterfeiting – industry sectors alongside well-informed customers, and national enforcement authorities.

In 2012, the WSC has established an Anti-Counterfeiting Task Force amongst the semiconductor industry associations of China, Chinese Taipei, Europe, Japan, Korea, and the United States, with the aim of promoting activities to fight counterfeiting, incl. training, awareness raising, and encouraging purchases from authorised sources. The WSC works closely with governments and authorities on policies and regulations, and encourages domestic, bilateral and multilateral counter-measures and enforcement activities. Such enhanced anti-counterfeiting cooperation activities at the industry level alongside government

⁴ Figures for 2013. Source: Organisation for Economic Co-operation and Development (OECD)–European Union Intellectual Property Office (EU IPO) (2016), *Trade in Counterfeit and Pirated Goods. Mapping the Economic Impact*, http://www.gacg.org/media/documents/201/041816_Mapping_the_Economic_Impact_en.pdf.

agencies, customs and law enforcement agencies is instrumental to identify and stop parties involved in manufacturing or trafficking in counterfeit goods.

About WSC

The World Semiconductor Council is a cooperative body of the world's leading semiconductor industry associations – consisting of the Semiconductor Industry Associations in China, Chinese Taipei, Europe, Japan, Korea and the United States – that meets annually to address issues of global concern to the semiconductor industry. The WSC also meets annually with the governments and authorities of the six regions to convey industry recommendations. The WSC is dedicated to the principle that markets should be open and competitive and works to encourage policies and regulations that fuel innovation, propel business and drive international competition in order to maintain a thriving global semiconductor industry.

More information on the WSC is available at <http://www.semiconductorcouncil.org>

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**Proposal for the amendments
of legal notes to HS Chapter 85 for Multichip-ICs
and for the corresponding HS explanatory notes**

Legal Notes

(b) 'Electronic integrated circuits' are:

- (1) monolithic integrated circuits in which the circuit elements (diodes, transistors, resistors, capacitors, inductances, etc.) are created in the mass (essentially) and on the surface of a semiconductor or compound semiconductor material (for example, doped silicon, gallium arsenide, silicon germanium, indium phosphide) and are inseparably associated;
- (2) hybrid integrated circuits in which passive elements (resistors, capacitors, inductances, etc.), obtained by thin- or thick-film technology, and active elements (diodes, transistors, monolithic integrated circuits, etc.), obtained by semiconductor technology, are combined to all intents and purposes indivisibly, by interconnections or interconnecting cables, on a single insulating substrate (glass, ceramic, etc.). These circuits may also include discrete components;
- (3) multichip integrated circuits consisting of two or more **interconnected** monolithic integrated circuits combined to all intents and purposes indivisibly whether or not on one or more insulating substrates, with or without leadframes, but with no other active or passive circuit elements.

Explanatory Notes**(III) Multichip integrated circuits.**

These consist of two or more **interconnected** monolithic integrated circuits combined to all intents and purposes indivisibly, whether or not on one or more insulating substrates, with or without leadframes, but with no other active or passive circuit elements.

Multichip integrated circuits generally come in the following configurations:

- Two or more monolithic integrated circuits mounted side by side;

- Two or more monolithic integrated circuits stacked one upon the other;
- Combinations of the configurations above consisting of three or more monolithic integrated circuits.

These monolithic integrated circuits are combined **and interconnected** into a single body and may be packaged through encapsulation or otherwise. They are combined to all intents and purposes indivisibly, i.e., though some of the elements could theoretically be removed and replaced, this would be a long and delicate task which would be uneconomic under normal manufacturing conditions. **The monolithic ICs may be interconnected to the terminals (outside world) of the component or among themselves or both in combination.**

Insulating substrates of the multichip integrated circuits may incorporate electrically conductive regions. These regions may be composed of specific materials or formed in specific shapes to provide passive functions by means other than discrete circuit elements. Where conductive regions are present in the substrate, they are typically relied upon as a means by which the monolithic integrated circuits are interconnected. These substrates may also be referred to as interposers or spacers when placed above the bottom-most chip or die.

Monolithic integrated circuits **are may be inter**connected by a variety of means, such as adhesives, epoxy resin, wire bonds, or flip chip technology.

The heading **excludes** film circuits consisting solely of passive elements (**heading 85.34**).

This heading **does not include** solid-state non-volatile storage devices, smart cards and other media for the recording of sound or of other phenomena (see **heading 85.23** and Note 4 to this chapter).

Except for the combinations (to all intents and purposes indivisible) referred to in Parts (II) and (III) above concerning hybrid integrated circuits and multichip integrated circuits, the heading also **excludes** assemblies formed by:

- (a) Mounting one or more discrete components on a support formed, for example, by a printed circuit;
- (b) Adding one or more other devices, such as diodes, transformers, or resistors to an electronic microcircuit; or
- (c) Combinations of discrete components or combinations of electronic microcircuits other than multichip-type integrated circuits.

Such assemblies are classified as follows:

(i) Assemblies which constitute a complete machine or appliance (or one classified as complete), in the heading appropriate to the machine or appliance;

(ii) Other assemblies, in accordance with the provisions for the classification of machine parts (Notes 2 (b) and 2 (c) to Section XVI, in particular).

This is the case, in particular, for certain electronic memory modules (e.g., SIMMs (Single In-line Memory Modules) and DIMMs (Dual In-line Memory Modules)). Those modules are to be classified by application of Note 2 to Section XVI. (See the General Explanatory Note to this Chapter).PARTS

Subject to the general provisions regarding the classification of parts (see the General Explanatory Note to Section XVI), parts of the goods of this heading are classified here.

Legenda:

Blue: Proposed changes to HS2017

Illustrative Examples of Enhanced Benefits for Trusted Traders

Introduction

AEO (Trusted Trader) Programs aim to enhance compliance and supply chain security coupled in parallel to bolstering efficient import and export processes. These programs require the implementation of appropriate systems and internal control programs by the participating companies. Due to complex and world-wide supply chains semiconductor companies have been investing very significantly to get certified as AEO.

However, WSC perceives that the benefits for AEO are not proportionate to the efforts and measures taken by the companies to comply with the AEO program and get certified. Benefits should be enhanced and become also more tangible, based on e.g. the lower risk profile of the semiconductor industry.

Further, WSC perceives that benefits differ in the different countries / GAMS regions through differing guidelines and implementation.

AEO programs should be developed and implemented consistently across GAMS regions and should consistent with the Article 7 of the WTO Trade Facilitation Agreement (TFA).

Illustrative examples (priorities)

1. Less physical inspections for trusted traders and less transaction-based customs audits for AEOs towards system based audits. Focus should be on the implementation of appropriate organizational measures, processes and internal compliance programs.

More in detail:

- Countries worldwide to implement – in a transparent way - uniform risk assessment criteria, resulting in a reduction of the number of physical inspections for AEO. This number should be significantly reduced in comparison with non-AEOs, especially for semiconductor AEOs, based on e.g. the risk profile of the semiconductor industry
- AEOs should benefit from a reduced number of audits (due to their compliance record and reliability which has to be proven upon application and under each re-validation)
- AEOs should benefit from expedite processing and release of shipments (imports and exports). The times should be significantly shorter than for non AEO. (E.g. automated release times from Customs IT systems).
- In case of a shipment (import or export) between two AEOs (in countries where an AEO MRA exists), there should be no physical inspections.

- Audits for semiconductor AEOs should be rather system based than transaction based.

2. Enhanced use of self-assessment and simplification of customs procedures; simplification of customs declarations, to be issued on a supplementary basis or monthly basis.

More in detail:

- Each AEO or AEO-type program should introduce the following additional simplification and harmonization measures
- Waivers or reductions of financial guarantees
- Deferment of payment of duties, e.g. on monthly basis
- Qualification for simplified procedures, e.g.
 - Transit simplifications, e.g. authorized recipient and consignor in EU
 - Special customs procedures (e.g. inward processing, end-use, bonded warehouse, etc.)
 - Simplified customs declarations (without presentation to customs, recording in the books, summarizing monthly supplementary declaration).
 - Central clearance, one stop shop
- Customs self-assessment

3. Worldwide level playing field for AEOs, i.e. same applied conditions and benefits ensuring the reduction and simplification of customs/import processes and procedures

More in detail:

- All above mentioned benefits can only work when a level of harmonization is achieved on risk assessment, customs processes, simplifications and agreed benefits.
- There should be a set of clear and specific international rules providing guidance to authorities in order to limit the possibility of diverging interpretations of AEO benefits and achieve a worldwide level playing field for AEOs.