European Semiconductor Industry Association

Position paper

Brussels, 5 November 2026

Multiannual Financial Framework 2028-2034:

For a resilient and market-driven microelectronics innovation ecosystem in Europe

Executive summary

Europe needs a strong and continuous funding framework for semiconductors and microelectronics across FP10/Horizon Europe and the European Competitiveness Fund, covering the full innovation chain from collaborative R&I to industrial deployment and scale-up. This must encompass both adequately funded collaborative R&I activities, including industry-driven bottom-up calls in the future Chips Joint Undertaking implementing the ECS SRIA, and measures supporting the objectives of the Chips Act 2.0. The future Chips JU must preserve this dual role, combining its established public-private partnership for collaborative R&I with the implementation of the Chips for Europe Initiative. ESIA therefore calls for sufficient and dedicated semiconductor funding in both Horizon Europe and the ECF, extending beyond the measures specifically established under the Chips Act 2.0.

To translate innovation into market uptake-ready technologies in the next European research and innovation programmes, ESIA calls on four strategic points to be fulfilled:

1- Position **Chips JU at the centre of Europe's R&I efforts**: maintain an independent, adequately funded and cross-sectoral Chips JU with a horizontal mandate spanning the full range of semiconductor technologies and application domains.
2- Establish **sufficient, dedicated and ring-fenced semiconductor funding envelopes** in both Horizon Europe and the ECF, covering the complete innovation chain.
3- **Align EU and national funding** to achieve scale and speed: create a continuous and coordinated funding pathway linking Horizon Europe, Chips JU, IPCEIs, the ECF and Chips Act instruments, with aligned procedures and timelines and clear complementarity.
4- **Protect European innovation without restricting globally integrated R&D**: replace rigid restrictions on IP, results and intra-group technology transfers with a beneficiary-centric, risk-based approach based on substantive European R&D, design and manufacturing activity and enforceable security safeguards

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Introduction

As Europe's central budget, the next 2028-2034 Multiannual Financial Framework (MFF) is poised to address and elevate the shared strategic priorities of Member States and Europe's high-tech industrial base in the coming years. Beyond assigning financial resources, the decisions made within the Framework will fundamentally shape Europe's capacity to generate, innovate and scale-up solutions in technology areas and sectors critical for our competitiveness. Among these, semiconductors continue to stand out as a bedrock for sustained Single Market and regional resilience.

As recently highlighted by the European Commission in the revised European Chips Act; **semiconductors are a foundational technology for Europe's digital transformation, industrial competitiveness, and strategic autonomy.** As strategic building-blocks, semiconductors and microelectronics enable advances across Europe's key application domains, including advanced manufacturing and industrial automation, energy, mobility and transport, healthcare, aerospace, security and defence. They also underpin computing, connectivity and artificial intelligence – including robotics and physical AI – providing the technological foundation for Europe's digital and industrial transformation, and green transition. Hence, the ability of Europe to pioneer and sustain investment in research and innovation (R&I) of semiconductors and microelectronics - across novel materials, advanced architectures, or heterogeneous integration - remains crucial to our region's future resilience. **This makes strengthening the technology area of semiconductors and microelectronics a vital European priority.**

This imperative is further underlined by the intensifying global competition in the sector, with entire regions channelling massive public and private investments into the semiconductor value chain (see annex). Nations in North America and East Asia are pursuing leadership in next-generation technologies, mature and leading-edge nodes, talent development, supply chain localisation and value chain control. For Europe, the challenge is therefore not merely to participate but to strategically differentiate our strengths and priorities where they matter the most. This requires leveraging Europe's unique innovation strengths in deep-tech research and equipment manufacturing, while fostering a highly collaborative research ecosystem backed by the MFF, that can accelerate the transition from lab to fab in high-value segments of the global semiconductor value chain.

To deliver on these priorities, **ESIA calls on the European Commission and Member States to position microelectronics and semiconductors as critical enabling technologies in the next research and innovation instruments Horizon Europe (HE) and European Competitiveness Fund (ECF). Accompanied by allocation of resilient budgets, stakeholder-conductive framework conditions and effective funding instruments, HE and ECF must be designed to respond to the needs of Europe's microelectronics industry.**

In this context, we would like to highlight the following priorities to ensure a stakeholder-centric, innovation-conductive research and innovation ecosystem delivers on the promises of the European Chips Act.

I. Position Chips Joint Undertaking at the centre of Europe's R&I efforts

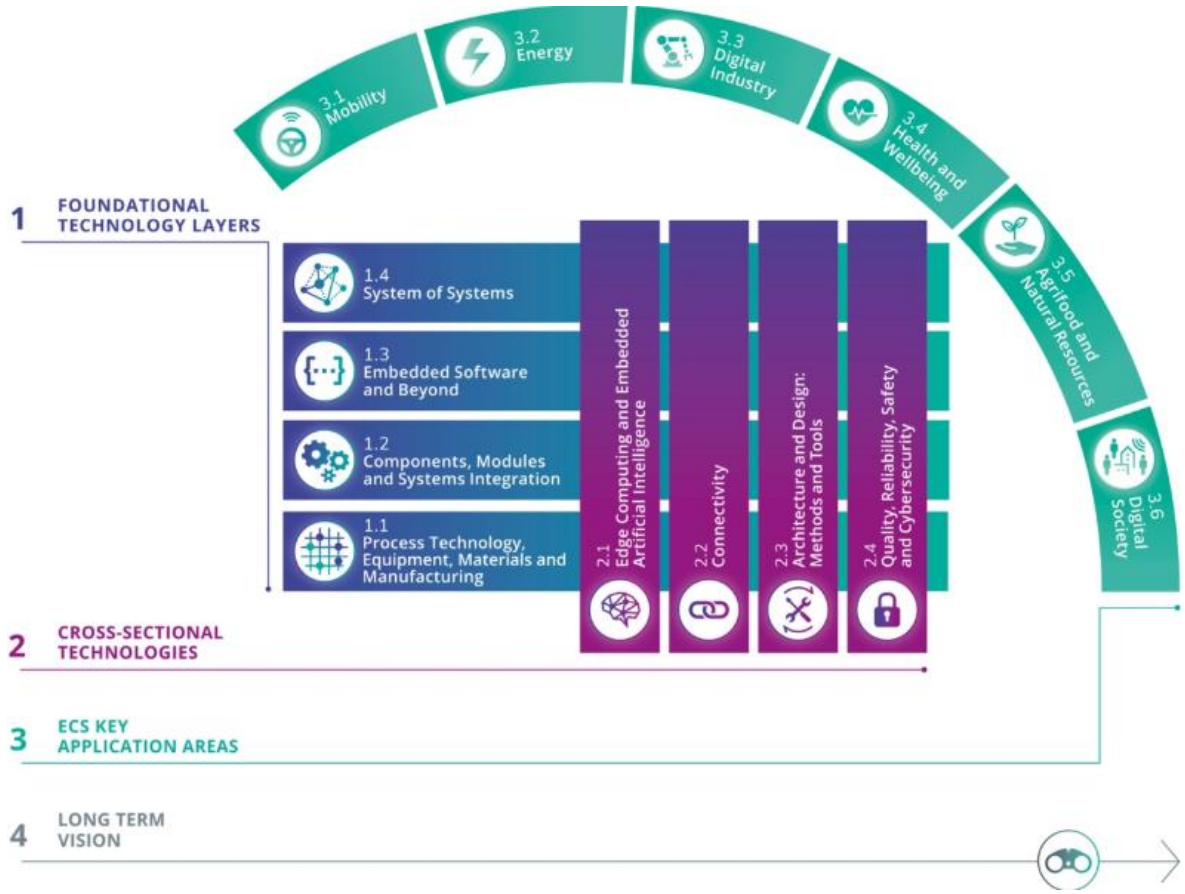
Semiconductor technologies are not only critical enablers of application verticals but also form the basis for technological enablers such as AI or quantum, driving transformative innovation across Europe's most critical sectors. This powerful synergy is not just improving existing systems and technologies but creating entirely new products and services across EU's competitiveness-critical industries such as automotive, manufacturing, energy or healthcare. As a horizontal enabling technology, semiconductors contribute directly to the success of multiple ECF objectives and should therefore not be constrained to a single funding silo.

Continuing this path, however, is not just a technical challenge; it demands agile tools and instruments designed for a transformative, cross-stakeholder innovation ecosystem. To accelerate the journey from discovery to market-ready technology, the European Commission's proposed Chips Joint Undertaking (Chips JU) must be firmly anchored with key industrial sectors and technology application domains.

Therefore, ESIA calls on the European institutions to position Chips JU – both a central mechanism for implementation of the EU Chips Act's Chips for Europe initiative and Europe's key public-private partnership for collaborative semiconductor research and innovation - as a horizontal high-tech enabler building on its track-record of success addressing a broad range of technological bottlenecks across critical European innovation segments. This dual role must be maintained in the future Chips JU, including sufficient scope and budget for collaborative, industry-driven bottom-up calls implementing the ECS SRIA.

An independent Chips JU needs to be maintained to ensure that technology innovation is not focused on the needs of a few selected application fields but on fit for reuse and uptake across domains for economies of scale.

If the discussed Digital Leadership portfolio (including chips, AI, cloud and connectivity) were to narrow the Chips JU's priorities to these technologies, it would risk limiting support for semiconductor innovation serving other application domains, including manufacturing, energy, mobility and healthcare. The Chips JU therefore needs a cross-sector mandate and sufficient autonomy to address these domains, irrespective of its portfolio allocation.



Electronic Components and Systems Strategic Research and Innovation Agenda (2026, under review)

II. Allocate globally competitive budgets and incentives for semiconductor R&D and industrial deployment

As a steadfast proponent of a resilient, competitive, and transformative European economy, ESIA recognises the progress made under the Irish Presidency of the Council and by the European Parliament towards negotiation positions for the next MFF.

For the semiconductor industry, the next MFF is more than just a budget; it is a powerful tool that shapes already today the confidence of the global industrial and investment community in Europe's competitiveness and resilience. It determines not only our future ability to translate technological breakthroughs into widespread innovation, but also our capacity to create new markets and cultivate an environment conducive to business growth and sustainable prosperity. Therefore, the upcoming MFF must not only anticipate and address future challenges within the Single Market but also rectify existing imbalances in the common EU policy-driven public spending – including persistent structural issues that will extend beyond the current budgetary cycle.

As pointed out in the Commission's recently published study on strategic digital technologies to determine areas for EU R&I beyond 2027: Europe maintains a strong research base in microelectronics, supported by world-class research institutions and strategic industrial players, holding globally leading positions in key R&I domains such as semiconductor equipment, power electronics and automotive-grade chips. **According to**

the study R&D intensity among European semiconductor firms - averaging ~15% of revenue, close to the US' 18.8% and double China's 7.6%[1], remains one of the highest in the world. This intensity of revenue spending must be further sustained and encouraged past the current MFF and innovation instruments, whether for future technological capabilities or to reinforce Europe's existing semiconductor industrial base. Public funding should complement this substantial private commitment by supporting collaborative research, shared infrastructure and the transition from research to industrial deployment across the innovation chain described below.

Europe needs a complete innovation chain for semiconductors, ranging from groundbreaking research in Horizon Europe, through collaborative and application-oriented R&I in the Chips Joint Undertaking, to industrialisation and scale-up supported through the ECF, IPCEI and the Chips Act 2.0. The future Chips JU must continue to provide dedicated opportunities for industry-driven collaborative research, including bottom-up calls implementing the ECS SRIA, alongside activities implementing the Chips for Europe Initiative.

ESIA urges policymakers to establish a sufficient, dedicated and ring-fenced semiconductor funding envelope both within the ECF, alongside adequate semiconductor funding under Horizon Europe to effectively pursue security of supply and demand objectives and stimulate the full spectrum of European semiconductor R&I and industrialisation. The funding envelope must encompass both collaborative R&I activities under FP10, including adequately funded bottom-up calls in the Chips JU, and measures supporting the objectives of the Chips Act 2.0, including strategic projects, ESTIs, demand instruments (including design porting and requalification), advanced packaging, mature and specialty technologies, product development and industrial deployment. Technologies enabled in Europe should be enabled to scale up in Europe. ESIA therefore supports the proposal of the European Parliament's ITRE Draft report, to scale the overall proposed budget of the ECF to EUR 257 billion and HEP to EUR 220 billion. These overall increases must be accompanied by the dedicated semiconductor funding envelopes called for above.

The ECF Regulation should explicitly link strategic projects designated under the Chips Act 2.0 to production-ramp-up and accelerated competitiveness actions and to the Competitiveness Seal. Projects and facilities already recognised or supported under the European Chips Act or IPCEI ME/CT should have a predictable pathway into ECF calls, subject to action-specific quality, security and Union-value-added criteria.

Only a European budget designed first and foremost with its beneficiaries in mind, will enable Member States' residing businesses to accelerate employment, technological resilience, and in many cases influence productivity factors that contribute to the growth of national GDP. These considerations should stand at the forefront of Member States' priorities for the upcoming trilogue negotiations.

[1] European Commission, Study on strategic technologies for the EU Research and Innovation Funding beyond 2027 – Annex 8, Technology Area Report, Microelectronics, 2026, available online.

III. Reinforce alignment of national and EU-level funding instruments to position semiconductor innovation at scale

In an era of intense global competition, a thriving, innovative semiconductor ecosystem is not a luxury but a strategic necessity. While significant public funds are being mobilised at both the EU and national levels to bolster this ecosystem, the full potential of these investments is being constrained by a lack of coordination.

The current landscape of funding instruments, though well-intentioned, is fragmented, leading to a duplication of efforts, administrative burdens for innovators, and a dilution of impact. This misalignment between national and EU-level initiatives impedes the industry's ability to achieve the necessary scale and velocity to compete effectively on the global stage. To maximise the return on public investment and accelerate our innovation output, it is imperative that we move beyond a collection of disconnected programmes toward a seamlessly integrated funding strategy.

To further the strengths of the EU's microelectronics ecosystem, **ESIA advocates for additional EU-funding opportunities to complement national investment initiatives such as IPCEI. To address fragmentation, such additional funding should be accompanied by coordinated EU and national funding procedures, aligned timelines and clear rules on complementarity, rather than adding another administrative layer.**

We therefore support Article 19 of the Commission's proposal for the European Competitiveness Fund to support specific projects integrated within IPCEIs, as well as follow-on industrial deployment of technologies developed through IPCEI ME/CT and Chips JU projects, based on their contribution to Union strategic priorities, such as the resilience of the Union, and on the ability of ECF financing to broaden participation, notably of SMEs, or broaden Member State coverage, as well as increase Union added value[2].

Only through alignment and complementarity of national investment initiatives and EU-funding instruments, can Europe deliver innovation at speed and scale. This alignment should provide a continuous funding pathway from research and innovation through pilot lines, pilot production and qualification to industrial ramp-up.

ECF work programmes should explicitly include semiconductor value-chain scale-up calls spanning foundries, advanced packaging, equipment, materials and design partners; ensure access for large enterprises as well as SMEs; permit relevant dual-use projects under both the Digital Leadership and Resilience, Security, Defence and Space windows; and ensure semiconductor industry representation in the ECF Stakeholder Board and relevant committee configurations.

[2] European Commission, Proposal on establishing the European Competitiveness Fund, 2025, available online.

IV. Reinforce Europe's competitive innovation strengths, not protectionist portfolios

Europe's strength in semiconductor R&D is not confined to its geographical borders. It is fundamentally global, built upon a network of companies with substantial R&D, design and manufacturing operations in Europe, whose facilities and fabs form globally integrated networks. Innovation in this sector is a fluid, collaborative process, with breakthroughs occurring seamlessly across all company-owned research, design, and manufacturing sites, regardless of their location.

Article 10 (2)(b) of the Commission's ECF proposal enables five-year transfer restrictions on certain operations, results or related access and use rights, including the granting of licences for ECF funding beneficiaries.

Such restrictions risk severing the vital arteries of an integrated European global innovation system.

Such an approach to the protection of European IP and investment results overlooks that a non-Union fab within the same corporate group may be an integral part of the innovation network supporting European R&D, design and manufacturing. Preventing the agile, cross-border deployment of intellectual property would artificially segment our own value chains and sub-optimise the innovation lifecycle.

This is why **ESIA advocates for a beneficiary-centric approach to IP, results, licences, use-rights protection and security from ineligible third country entities by requiring ECF-beneficiaries to certify their compliance with all security and IP protection measures specified in the grant agreement for a period of up to 5 years after the funding award for the relevant action. Failure to meet these security obligations should result in penalties detailed in the specific award procedure document.**

Such a beneficiary-centric approach would allow ECF-funding recipients to ensure organisation-wide compliance and maintain the innovation agility required to succeed in the fast-paced global semiconductor market. Rather than imposing rigid restrictions that hinder innovation, this model empowers companies to leverage their own comprehensive, worldwide security and IP protection infrastructures and talent to leverage European IP to support manufacturing in Europe.

For ESIA, such an approach places accountability where it is most effective—with the beneficiary who best understands its own systems and innovation security risks. To safeguard the Union's strategic interests, this accountability should be backed verifiable safeguards for intra-group transfers, monitoring rights for the granting authority and enforceable sanctions, while enabling beneficiaries to use their global networks to strengthen R&I and manufacturing in Europe.

Eligibility should therefore be based on substantive R&D, design and manufacturing activity, economic contribution and enforceable Union security safeguards, rather than ultimate ownership. Facilities already assessed under the European Chips Act or IPCEI ME/CT should not face duplicative ECF ownership screening unless control or risk has materially changed.

Annex: International comparison of Government support for microelectronics

Support instrument	Japan	United States	South Korea	China	European Union
Direct state aid / grants	• Large fab and R&D grants • Strategic support for *TSMC Kumamoto* and *Rapidus*	• CHIPS Act manufacturing incentives • Dedicated R&D, defence, security and workforce funds	• Semiconductor investment funds • Public investment in memory, packaging and clusters	• Central and local grants • National and provincial funds • Rescue support for strategic firms[3]	• Chips Act and IPCEIs • National aid for FOAK fabs, R&D, pilot lines and industrial scale-up[4]
Tax support	• High R&D tax credits • Enhanced credits for strategic technologies and joint research	• Advanced Manufacturing Investment Credit • Federal R&D and state-level tax incentives	• K-Chips investment and R&D credits • Higher rates for SMEs	• Tax holidays by technology node • Accelerated depreciation and R&D incentives	• Member-State R&D and investment relief • Accelerated depreciation and CAPEX relief under discussion[4]
Preferential finance / public equity	• Government-backed financing • Long-term public-private investment frameworks	• Federal loans and loan guarantees • Additional state and local financing	• Low-interest and policy-bank loans • Sovereign wealth fund for strategic industries	• Large-scale below-market lending • Public equity through state investment funds[5]	• EIB, InvestEU, and promotional-bank finance • Loans and guarantees complement grants[4]
Infrastructure, land and utilities	• Publicly supported sites and utilities • Streamlined approvals for strategic fabs[4]	• Site preparation and infrastructure • Utilities and workforce measures in state/local packages	• State-funded utilities in semiconductor clusters • Special-zone infrastructure	• Cheap or free industrial land • Subsidised utilities, industrial parks and upstream inputs[3]	• Co-financed energy, water, waste and transport infrastructure • Some national energy-cost relief[4]
Market access / demand support	• Resilience-oriented procurement • Long-term industry partnerships and domestic-capability focus[4]	• Buy American rules • Tariffs and export controls reinforce onshoring[4]	• Domestic production and localisation incentives • Cluster-based demand and supply-chain policies	• Procurement preference and local-content rules • Domestic substitution and protected home-market access[3]	• Limited procurement and demand-side tools • Defence and critical-infrastructure preferences under debate[4]
Regulatory / administrative support	• Structured government-industry partnerships • Faster approvals for strategic projects[4]	• Dedicated CHIPS Program Office • Permitting remains partly state-specific[4]	• Special Semiconductor Act • Special-zone rules shorten approvals and environmental procedures	• Fast local execution • Industrial-zone administration and whole-of-government coordination[3]	• Strategic-project status and permitting facilitation • Procedures remain fragmented and comparatively slow[4]
Overall policy pattern	• Targeted grants • Tax incentives and strategic alliances	• Large grants and tax credits • Loans, procurement and trade/security measures	• High tax incentives • Cheap finance and cluster infrastructure	• Broadest instrument mix • Grants, tax relief, cheap finance, land, utilities and market protection[5]	• Grant-led model with strong R&I support • Less harmonised indirect cost relief and demand instruments

[3] MERICS (2025), Beyond Overcapacity, pp. 14-16; MERICS (2026), China's Economic Security Offensive, pp. 12-14.
[4] ZVEI & Strategy& (2024), From Chips to Chances, chapter 3; ZVEI/FME & Strategy& (2026), Europe's Semicon Business Case, chapters 2-4.
[5] OECD (2026), OECD MAGIC Database of Industrial Subsidies, pp. 8-12 and 31-33.

For further information:

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ABOUT ESIA

The European Semiconductor Industry Association (ESIA) is the voice of the semiconductor industry in Europe. Its mission is to represent and promote the common interests of the Europe-based semiconductor industry towards the European institutions and stakeholders in order to ensure a sustainable business environment and foster its global competitiveness. As a provider of key enabling technologies, the industry creates innovative solutions for industrial development, contributing to economic growth and responding to major societal challenges. Being ranked as one of the most R&D-intensive sectors by the European Commission, the European semiconductor ecosystem supports approx. 200.000 jobs directly and up to 1.000.000 jobs indirectly in systems, applications and services in Europe. Overall, micro- and nano-electronics enable the generation of at least 10% of GDP in Europe and the world.