EECA ESIA

European Semiconductor Industry Association

Intermediate Status Report of the Progress towards the Reduction of Perfluorocompound (PFC) Emissions from European Semiconductor Manufacturing

2006

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European Semiconductor Industry Association

The European Semiconductor Industry Association (ESIA), part of the European Electronic Component manufacturers' Association (EECA), represents the European-based manufacturers of semiconductor devices. The semiconductor industry provides key enabling technologies at the forefront of the development of the digital economy. The membership supports over 100,000 direct jobs in a consumption market valued at around €31.8bn in 2006.

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1. Introduction

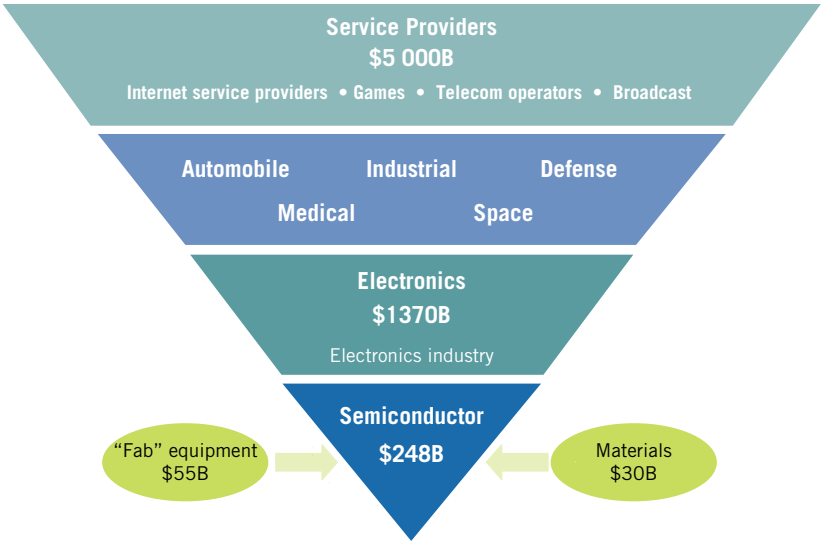
This intermediate status report demonstrates the proactive voluntary approach of the semiconductor industry to reduce its environmental footprint and address climate change. It outlines the European semiconductor industry's actions to reduce the emissions of perfluorocompounds (PFCs), and gives an update of the progress of the European industry towards achieving the European Semiconductor Industry Association (EECA-ESIA) reduction goal. The EECA-ESIA goal as outlined in the *Memorandum of Agreement (MOA) of EECA-ESIA* is to reduce by 2010 the absolute PFC emissions of the European industry by 10% below the baseline year of emissions in 1995. If no progressive action and investments had been undertaken by the European industry to reduce emissions, these would have increased significantly more than 1995 levels under a business as usual scenario. The report is being published in accordance with section II B of the *MOA*. This regional goal forms part of the overall global semiconductor industry's proactive response to reduce PFC emissions on a worldwide basis by 10% by 2010. The global goal is coordinated through the World Semiconductor Council (WSC), with each regional semiconductor trade association in Japan, Korea, America, and Taiwan having individual goals to contribute to the worldwide emission reduction efforts. It is important to outline that – through the WSC – the semiconductor industry was the first industry to align globally and establish a worldwide greenhouse gas emission goal which goes beyond the targets established by the Kyoto protocol for Annex 1 countries.

The EECA-ESIA goal is to reduce by 2010 the ABSOLUTE PFC emissions of the European industry by 10% below the baseline year of emissions in 1995. If no progressive action and investments had been undertaken by the European industry to reduce emissions, these would have increased significantly more than 1995 levels under a business as usual scenario.

The semiconductor industry features a number of distinct characteristics that position it uniquely in the European economy;

- High intensity of R&D spending (up to 20% of annual revenues) and the high level of capital investments for a new semiconductor plant ($2.5-3bn)
- The semiconductor industry is a technology enabler. Semiconductor products form an increasingly vital part of a whole range of consumer products ranging from electronic devices and systems (e.g. PCs, mobile phones, TV sets) to solutions and services (e.g. Internet providers, telecom operators, broadcasting services, automotive industry).
- Revenues in the overall microelectronics industry have a multiplier effect on other major downstream sectors where electronic content is central (figure 1). From a worldwide semiconductor consumption market of €197bn/$248bn in 2006, the European semiconductor consumption market was valued at approximately €31.8bn/$39.9bn.

Figure 1



Various sources

The semiconductor industry is an extremely minor contributor to the overall emissions of greenhouse gases (GHG) by sector in Europe. Based on 2003 European Union GHG emission data (4180 million tonnes CO_2 equivalents)[1], the semiconductor sector emissions accounted for .05% of the total. Nevertheless, the industry is highly committed to its environmental responsibilities and to proactively lowering its emissions. The information in this report has been compiled with the cooperation of the semiconductor manufacturing facilities operating in Europe. It reflects information available through January 2006. It is not intended to give an exhaustive list of all technical PFC emission reduction activities ongoing.

2. Use of perfluorocompounds (PFCs) in semiconductor manufacturing processes

To produce semiconductor devices, the semiconductor industry requires gaseous fluorinated compounds, silanes, doping and other inorganic gases. Wafers consist of high-purity silicon and are the basic building blocks for all semiconductor components. The PFCs used in semiconductor manufacturing process are: hexafluoroethane (C_2F_6), octofluoropropane (C_3F_8), tetrafluoromethane (CF_4), octofluorocyclobutane (c-C_4F_8), nitrogen trifluoride (NF_3), sulfur hexafluoride (SF_6) and hydrofluorocarbons such as trifluoromethane (CHF_3).

Table 1 - Greenhouse gases: GWPs and atmospheric lifetimes

Gas Compound	Chemical Formula	CAS number	GWP_{100}**	Atmospheric lifetime (years)*
Hexafluoroethane	C_2F_6	76-16-4	11900	10000
Octofluoropropane	C_3F_8	76-19-7	8600	2600
Tetrafluoromethane	CF_4	75-73-0	5700	>50000
Octofluorocyclobutane	c-C_4F_8	115-25-3	10000	3200
Nitrogen Trifluoride	NF_3	7783-54-2	10800	>500
Sulfur Hexafluoride***	SF_6	2551-62-4	22200	3200
Trifluoromethane	CHF_3	75-46-7	12000	260

* European Commission Report on *Progress Towards Achieving the Community's Kyoto Target; Com 2005 655 Final*

** GWP-Global Warming Potential of the gas relative to carbon dioxide, for a time horizon of 100 years. These global warming potential values come from the Intergovernmental Panel on Climate Change, *Climate Change 2001: The Scientific Basis* (Cambridge, UK: Cambridge University Press, 2001). These are the current values used for calculating the semiconductor reporting in Europe.

*** Sulfur Hexafluoride is included in the basket of gases. This report refers to 'perfluorocompounds' and not just perfluorinated carbon compounds (PFCs).

Essentially, these high-purity gases are used in a number of different process steps.

1. PFCs are used as etching gases for plasma etching. The gases etch the submicron patterns on metal and dielectric layers of advanced integrated circuits. In addition, SF_6 decomposed by the plasma allows the etching chambers to be cleaned.
2. The fluorinated compounds are also used to accurately perform a rapid chemical cleaning of Chemical Vapor Deposition (CVD) tool chambers. When the silicon and silicon based dielectric layers are being applied, a deposit remains in the CVD chamber. To ensure that the wafers do not become contaminated by these deposits, the chambers are cleaned at defined intervals, avoiding frequent mechanical wet cleanings.

1 European Commission Report on *Progress Towards Achieving the Community's Kyoto Target; Com 2005 655 Final*

3. In the wafer testing process stage, SF_6 is used as insulator for power device testing. Power devices are used for automotive applications to simulate the real device working conditions which are essential to prove semiconductor device reliability. The SF_6 reuse concept can allow SF_6 to be used in an environmentally friendly manner and to be kept in a closed cycle.

PFCs have been used in semiconductor fabrication plants because they provide a uniquely effective process performance when etching and are a safer, more reliable source of fluorine, which is required for cleaning certain deposition process chambers. Manufacturers of semiconductor devices have been able to reduce PFC emissions by taking a number of actions including process optimization, use of alternative chemicals, employment of alternative manufacturing processes and improved abatement systems. However, the use of PFC gases in these processes is crucial to the production of semiconductor devices, as there are no effective substitutes that could be utilized.

3. Emission reduction technology development

The semiconductor industry employs a hierarchy in the development of PFC emission reduction technology. This is structured around the pollution prevention concepts of *reduce*, *replace*, *re-use/recycle*, and *abate*. These development areas are:

1. **Process optimization/alternative processing** - ***reduces the amount of PFCs that are used and emitted*;**
2. **Alternative processing chemistries – *reduces or eliminates emissions*;**
3. **Capture/recovery – *re-uses or recycles PFCs*;**
4. **Abatement – *reduces or eliminates PFCs emissions*.**

The use of PFC gases in these processes is crucial to the production of semiconductor devices, as there are no effective substitutes that could be utilized.

3.1 Process optimization

Process optimization continues to focus primarily on CVD chamber cleans because they have historically been the largest source of PFC emissions. Furthermore, they occur in the absence of wafers and can be optimized without negatively affecting product yield. The PFC gases used in CVD chamber cleans include C_2F_6 and CF_4 in older (pre-1999) manufacturing equipment, as well as C_3F_8, C_4F_8, C_4F_8O (octafluorotetrahydrofuran) and NF_3 that are lower emitting C_2F_6 replacement chemistries. These last substances have become more common since the years 1999-2000.

Based on 2005 emission data collection, C_2F_6[2] continues to be the primary chamber clean gas and currently makes up the majority of semiconductor PFC emissions. However, in terms of amounts purchased, NF_3,with a lower environmental impact, is fast replacing C_2F_6. In process optimization, endpoint detection or extractive metrology are used to monitor emissions and provide clean end point times that are minimized by adjusting process parameters such as chamber pressure, temperature, plasma power, cleaning gas flow rates, and gas ratios in the case of mixtures. Cleans are optimized to minimize gas consumption, thereby resulting in lower cost of ownership (COO) due to decreased gas usage. Process optimization can yield emissions reductions of 10-56%[3] compared with non optimized processes. Moreover, it is a low cost emission reduction option with potential process throughput benefit. Because of industry growth, optimization by itself has not achieved the levels of emission reduction the industry needs to meet the 10% goal; however, optimization effectively reduces emissions in older fabs and ensures that new chamber clean processes minimize gas consumption and operate efficiently.

2 A. D. Johnson, R. V. Pierce, M. I. Sistern, M. Kencel, R. Sward, and H. Winzig, Semiconductor International, 27 (3), p.57 (March, 2004).
3 C. Allgood, S. Hsu, B. Birmingham, and J. Soucy, Proceedings of the SEMICON Southwest 'A Partnership for PFC Emissions Reductions' Seminar, paper #9 (2000).

3.2 Alternative processing chemistries

Replacement of the original process with a new and lower emitting process, is a technology area which has undergone significant development in recent years. The industry has developed remote plasma clean technologies to replace in-situ C_2F_6 and CF_4 chamber cleans. Remote cleans dissociate NF_3 into fluorine ions or atoms in a remote plasma and then feed the F ions/atoms into the process chamber to remove silicon-based residues. Remote cleans convert NF_3 at 95-99% utilization efficiency, and semiconductor companies have adopted remote plasma technology for chamber cleans across their advanced 200mm and 300mm CVD equipment line. Some companies have developed remote plasma technologies utilizing NF_3 or other PFC chemistries that can be retrofitted to certain older CVD chambers. When compared to the original carbon based PFC chamber cleans that they replace, retrofitted remote cleans result in >95% PFC emissions reduction and improved tool utilization through; reduced clean times, reduced wet clean frequency, improved mean time between failures (MTBF), reduced chamber parts costs and improved yield through reduced defects.

While replacement of high GWP gases with lower or non-GWP gases is generally preferable, it has not proven feasible in most plasma etch applications. Processing requirements for high aspect ratio plasma etching continue to become more stringent, requiring both fluorine to etch and the right carbon to fluorine ratio to ensure anisotropic etching. While a significant amount of research has been done on alternative etchants such as iodofluorocarbons, hydrofluorocarbons, and unsaturated fluorocarbons, many of these chemicals are not viable alternative etchants in a manufacturing environment due to excess polymerization, lack of etch selectivity, difficulties in delivering gases to the process chamber, and potential increased employee exposure risks. An exception is hexafluoro-1,3-butadiene (C_4F_6) for oxide and low-k etching where high selectivity for silicon is required in the presence of nitride or other films with high aspect ratios, thinner resists and less etch resistant resists. In these cases, C_4F_6 replaces CF_4, CHF_3, and C_4F_8[4]. With an atmospheric lifetime <1 year and utilization efficiency >95%, PFC emission reductions >90% compared to conventional gases can be achieved; however, also in this case some CF_4 is formed and emitted.

The industry has developed remote plasma clean technologies to replace in-situ C_2F_6 and CF_4 chamber cleans.

It is important to note that, for any alternative chemistry that results in decreased PFC emissions, emissions of F_2, HF and other by-products may not correlate; fluorocarbons generate other PFCs and COF_2 while NF_3 results in increased F_2, HF, and NO_x emissions. Reducing PFC emissions should be balanced with other Environmental Safety and Health (ESH) concerns. For example, NF_3 in the combination with deposition gases, such as SiH_4 may be explosive when not sufficiently diluted. In fact, in a multi-chamber configuration, it is highly probable that when one chamber is in deposition mode, in another one the chamber clean is running. Japanese industries are proposing - as replacement gases for cleanings - gases such as ClF_3 and COF_2, which are very reactive, corrosive and toxic. Very strict controls and handling procedures must be in place to ensure a safe working environment and minimize emissions to the atmosphere.

3.3 Capture/Recovery

Several semiconductor manufacturers and suppliers conducted alpha and beta evaluations of PFC capture/recovery systems which could be installed as a central, building-wide means for handling PFC emissions. No evaluation resulted in successful re-use of PFC; all were deemed to be too costly to implement. As NF3 based cleans proliferate, large building-wide capture/recovery systems become less cost effective due to the reduced volume of PFCs available for recovery. To date, no semiconductor facility has implemented centralized capture/recovery technology.

4 F. Fracassi, R. d'Agostino, E. Fornelli, F. Illuzzi, T. Shirafuji, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, Volume 21, Issue 3, pp. 638-642, May 2003.

Currently the recovery technology seems to be favourable for SF_6. In addition to plasma etch processes, SF_6 can be found in specialized processes such as IC testing and wafer thinning where it is used in large volume. In this case small capture/recovery systems appear to be appropriate for niche, single PFC, high volume processes.

3.4 Abatement

Significant developments have occurred in the area of PFC abatements, with the development of new technologies and the commercialization of many new systems[5]. The industry has favoured point-of-use abatement over centralized end-of-pipe (EOP) abatement for PFCs, believing that it is more effective to abate close to the source and, thus, prior to dilution. Most abatement technologies can be applied to PFC emissions from both etch and CVD processes, although several companies have developed plasma abatement systems specifically for etch chamber emissions. These are typically installed prior to the vacuum pump (i.e., the foreline) to avoid dilution of the stream with pump-purge N2.

As noted earlier, fluorocarbons will generate CF_4 and possibly C_2F_6 and C_3F_8 when used in plasma processes. Additionally, the use of any fluorine-containing compound in the presence of carbon in a plasma process, such as for organic low-k deposits in a chamber, will result in the formation of some quantity of CF_4. Performance of abatement systems varies greatly depending on a variety of abatement and process parameters such as temperature, PFC inlet concentration, flow rate, overall inlet stream composition, etc. In addition, consumables, maintenance, and utilities will have a significant impact on COO.

The age, size and infrastructure of a fab are the factors that have the greatest impact on the applicability of PFC emission reduction technology.

4. Investments in technologies & R&D

The age, size and infrastructure of a fab are the factors that have the greatest impact on the applicability of PFC emission reduction technology. For instance, older fabs process smaller wafers, are typically smaller in size, and may have space and infrastructure constraints to allow the installation of reduction technologies. Moreover, manufacturers of the process tools in older fabs are typically no longer supporting those tools with new process development. ESIA member companies were surveyed to determine the technologies that they are implementing to reduce emissions. The following table summarizes the PFC emissions reduction options the industry is applying to fabs processing various wafer sizes and different fab age. As already mentioned in the paragraph 3.1, new technologies were introduced on both 200 and 300 mm equipment after the year 1999.

Table 2: PFC Emissions Reduction Options

Tool Type	≤150mm fabs	Old Technology 200mm	Advanced 200mm and 300mm
CVD	Fab Decommission Process Optimization Endpoint Detection Alternative Chemistries Limited Abatement	Process Optimization Endpoint Detection Remote NF3 cleans Alternative Chemistries Abatement	NF3 Based Cleans F2 Cleans Endpoint Detection Abatement
Etch	Fab Decommission	Limited Abatement Limited Capture/Recovery	Alternative Chemistries Abatement Limited Capture/Recovery

5 *Reduction of perfluorocompound (PFC) emissions: 2005 State-of-the- Technology Report,* Technology Transfer #05104693A-ENG, International SEMATECH, (2005)

4.1 Cost effectiveness of emission reduction investments

The ESIA PFC emissions reduction goal comes with significant cost implications for all companies involved in the project[6]. In comparison with many other industry sectors, the European semiconductor industry is often confronted with high marginal costs to reduce a small amount of emissions. The costs are high in respect of the absolute reductions achieved, since the PFC emissions by the semiconductor industry are only a very minor aspect of overall industry GHG emissions.

As mentioned above in section 3, only process optimisation is cost-effective. It affords lower gas consumption, and therefore, lower emissions and may lead to throughput benefits. However, to achieve this, the processes must be optimised and (partly) re-qualified and this requires significant engineering resources.

The implementation of alternative processes and, in particular, of abatement measures has involved significant investments to be made by the European semiconductor industry.

These investment costs include:

- Qualification costs for alternative processes (every process must be released from production).
- Hardware and installation costs (dedicated process tool configurations, abatement tools).
- Infrastructure costs (gas supply, energy supply, downstream effluent treatment). Space requirements and special safety precautions may significantly enhance these costs.
- Running costs (abatement systems, etc.).

There may be a large variation in costs. In the case of a new fab the cost impact will be less than in the case of an already existing fab. This is because new production facilities can be built according to the newest insights, whereas for older fabs, the implementation of measures and retrofits interferes with running production, and sometimes the existing infrastructure poses problems leading to disproportionate costs.

... the European semiconductor industry is often confronted with high marginal costs to reduce a small amount of emissions.

5. Impact of industry changes on emissions

The industry is currently undergoing significant changes that are likely to have an impact on PFC emissions levels. These changes include development and implementation of new chamber clean processes and chemistries, increased use of plasma etching and adoption of new etch gases, development of new materials and processes, and larger wafers to manufacture the advanced semiconductor devices.

5.1 Etch

The switch from 200 to 300mm equipment has resulted in a 1.5-2x increase in etch PFC consumption per wafer pass. However, the increased usage is less than would be expected based on the 2.25x increase in wafer area.

The increase in microprocessor metal layers has led to an increase in back end PFC usage. Due to requirements for higher selectivity to resist and underlying films, c-C_4F_8 and C_4F_6 are now being used much more extensively for dielectric etching, replacing CHF_3 and CF_4. Both chemistries generate C_2F_4, CF_4, C_3F_8, C_2F_6, CHF_3 and some

6 Final Report on the European Climate Change programme prepared on behalf of the European Commission by Jochen Harnisch and Ray Gluckman, 2001,page 43

C_4F_8. When using C_4F_6 instead of c-C_4F_8[7] for organosilicate glass and oxide etching, equivalent process performance has been demonstrated to lead to 65%-82% PFC emissions reduction.

As device line and contact sizes are scaled, the aspect ratio remains the same. Therefore, sometimes films are becoming thinner and etch times shorter, resulting in decreased PFC usage. However, the selectivity requirements are also becoming more critical with the thinner layers and required process changes may result in increased PFC consumption over time. The impact of ultra low-k dielectrics on PFC emissions cannot be ascertained at this time because it is too early in their development stage.

In the front-end, integrations - using multiple spacers and sometimes multiple polysilicon layers - have resulted in increased PFC usage. As high-k dielectrics and gates are implemented, increased etching could result in further increases in PFC consumption.

In recent years, semiconductor tool suppliers have evaluated in-situ cleans or dry cleans for etch tools to maximum tool uptime and increase mean time between wet cleans (MTBC). While oxygen can be used to clean organic by-products of the resist from the chamber walls, fluorine-containing gases are required to remove silicon-based residues. The use of in-situ cleans is likely to result in increased PFC emissions from etch tools.

In conclusions, etch will become a significant source of 300mm PFC emissions.

5.2 Future technologies that may impact PFC emissions

Atomic Layer Deposition (ALD) is increasingly used in the industry to deposit back end copper barriers and seed layers. In the front-end, ALD is being used to deposit metal gates and high-k dielectrics. These materials replace films that formerly were deposited by diffusion processes that did not have PFC chamber cleans. In-situ and remote plasma NF_3-based chamber cleans are currently in development to replace ex-situ cleans, which require that the chamber be taken down so that parts can be removed. Non-PFC chemistries are also being evaluated for in-situ or remote plasma chamber cleans.

Finished semiconductor wafers contain multiple integrated circuits called die. The finished die are cut, packaged and then sent to manufacturers to integrate into products such as cell phones, computers, personal music players and automobiles. The shrinking size of electronic products requires that packaged integrated circuits be reduced in thickness and footprint. Thin IC packages require thinner die; additionally, fully depleted silicon on insulator (SOI) used for low power, high speed devices also requires thinning of SOI wafers. One of the major methods for reducing die thickness is the atmospheric downstream plasma (ADP) etching and obviously this etching step requires use of PFCs.

5.3 Wafer size changes

The change with the largest impact on PFC emissions over time is increasing wafer size and the corresponding advanced processing technologies. Older technology ≤150mm wafers constituted the bulk of wafer demand in 1995. PFC emissions increased between 1995-2000 as first generation 200mm fabs, using predominantly C_2F_6 cleans, ramped up; 200mm wafers became the predominant wafer type by 2000. As advanced 200mm and 300mm wafer fabs began ramping in 2001-2004, the normalized rate of emissions (PFC emitted/cm^2) decreased, most likely due to use of alternative gas based chamber clean processes. Advanced 200mm and 300mm fabs will account for approximately 70% of semiconductor manufacturing wafer demand in 2010[8].

7 *Unsaturated Fluorocarbon Etching of Oxide and Low-k Films in High Density and Medium Density Toolsets* Technology Transfer #02014234A-TR, R. Chatterjee, R. Reif, T. Sparks, V. Vartanian, L. Mendicino, B. Goolsby, Jan. 2002.

8 Same as reference *5*

6. Progress towards the EECA-ESIA 2010 reduction goal

6.1 Emission calculation methodology

The methodology used for emission calculation was suggested in the 1996 *IPCC Guidelines for National Greenhouse Gas Inventories, revised in 2001* and currently under revision. The publication of the 2006 version is forecast within the end of the year. Semiconductor companies adopted almost unanimously the Tier 2C calculation method for their emissions.

Equation for PFC Calculations

Emissions for PFC_i = PFCi*(1-*h*)[(1-C_i)(1-A_i)*GWP_i + B_i*GWP_{CF4}*(1-A_{CF4})]

where

h = fraction of gas_i remaining in container (heel)
PFC_i = purchases of gas_i = kgs_i
kgs_i = mass of gas_i purchased
GWP_i = 100 yr global warming potential of gas_i
C_i = average utilization factor of gas_i (average for all etch and CVD processes) = $1\text{-}EF_i$
EF_i = average emission factor of gas_i (average for all etch and CVD processes)

B_i = mass of CF_4 created per unit mass of PFC_i transformed
A_i = fraction of PFC_i destroyed by abatement = $a_{i,j}*V_a$
A_{CF4} = fraction of PFC_i converted to CF_4 and destroyed by abatement = $a_{CF4}*V_a$
$a_{i,j}$ = average destruction efficiency of abatement $tool_j$ for gas_i
a_{CF4} = average destruction efficiency of abatement $tool_j$ for CF_4
V_a = fraction of gas_i that is fed into the abatement tools

Table 3 - Emission factors stated in 2001 guidelines

	CF_4	CHF_3	C_2F_6	C_3F_8	NF_3	SF_6	C_4F_8
Tier 2C Constant *1-Ci*	0.8	0.3	0.7	0.4	0.2	0.5	0.3
Tier 2C Constant B	0	0	0.1	0.2	0	0	0.1
Tier 2C Constant *A* (Abatement)	0.9	0.9	0.9	0.9	0.9	0.9	0.9

It is important to note that some figures obtained by adopting these factors result in an overestimation compared to actual emissions. For example for NF_3 the utilization factor currently adopted is 80%, while as widely explained in the previous paragraphs, in the new generation tool it is around 99%.The revision of the formula will take into account these process changes[9].

6.2 Emission reduction achievements

In the figure 2 the European emission data collected starting from 1995 are reported, the yearly data are fractioned for each gas type used. By analyzing them it can be appreciated that:

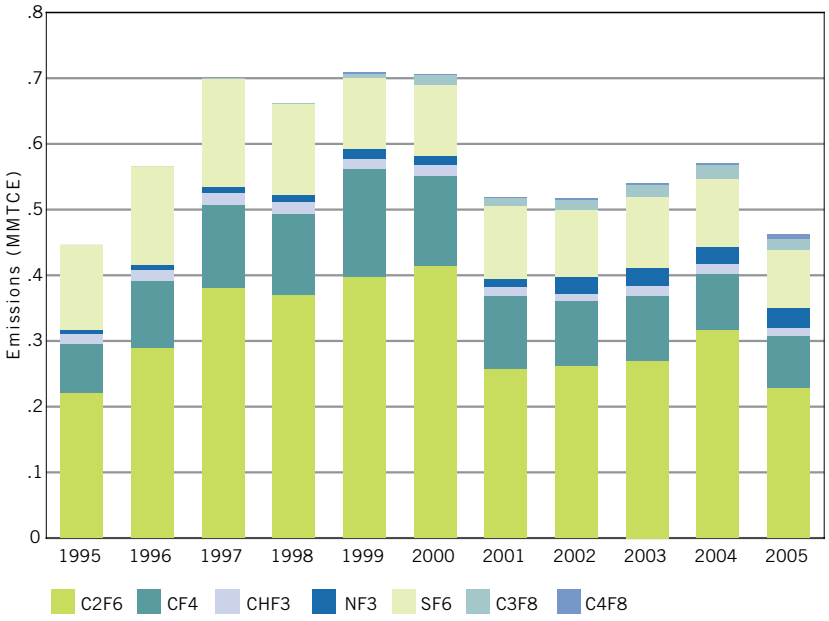
- The ESIA Partners have achieved significant reductions of PFCs between 2001 and 2005 in comparison with their peak level emissions.
- ESIA reductions have been achieved through implementation of process optimization and alternative processes, use of alternative chemistries, and installation of abatement. Some older technology fabs have been closed while newer technology fabs have been built which utilize lower emission technologies and abatement.

9 IPCC Electronics Industries GHG Emissions Estimating Draft, 2006

- Looking at the different gases used it is evident that NF_3 emissions have increased over time, reflecting ramp up of advanced 200mm and 300mm manufacturing in Europe.
- C_2F_6 makes up the bulk of ESIA emissions and, while C_2F_6 emissions had appeared to peak in 1999 and then declined from 2000-2005 with a slight increase in 2004.

In conclusion, the aggressive efforts which are being implemented to reduce C_2F_6 emissions from existing fabs should allow ESIA to meet the 10% reduction goal.

Figure 2 – European IC company emission data from 1995 to 2005



The aggressive efforts which are being implemented to reduce C_2F_6 emissions from existing fabs should allow ESIA to meet the 10% reduction goal.

Another very positive result achieved by the European companies is a continued decrease in the normalized emissions NER (MMTCE/square meter of wafer demand – *Million Metric Tonnes of Carbon Equivalent)*. This reduction in normalized emissions means that the industry has consistently reduced PFC emissions per square meter of silicon since 2001 (as illustrated in figure 3). Assuming this trend continues emissions can be projected through 2010, and using a linear extrapolation it can be said the goal is going to be reached.

Figure 3 – European normalised emissions have continued to decrease. A comparison between actual European emissions and projected emissions if no reduction options had been implemented.

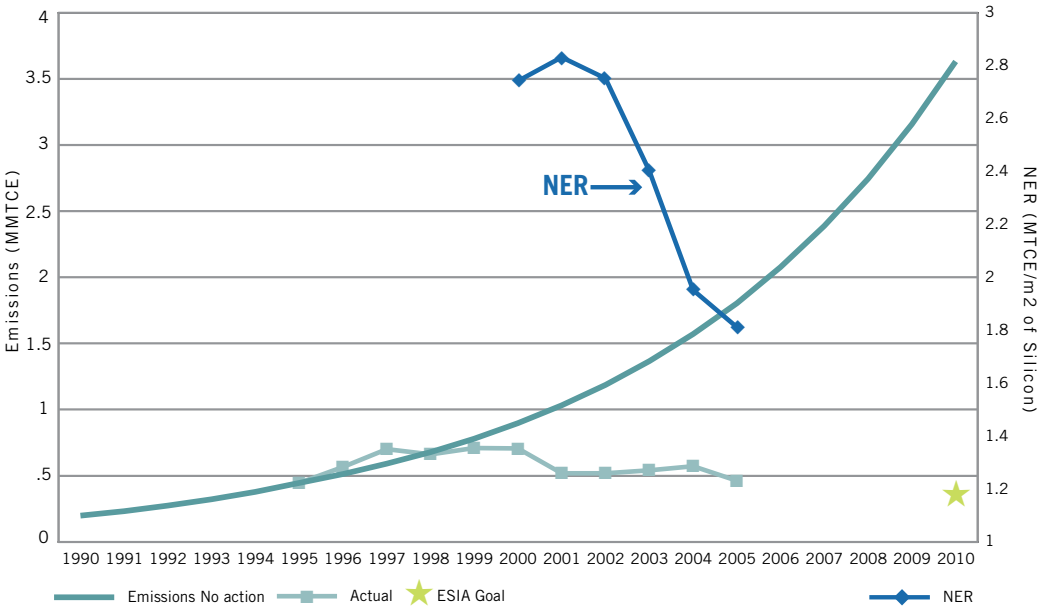
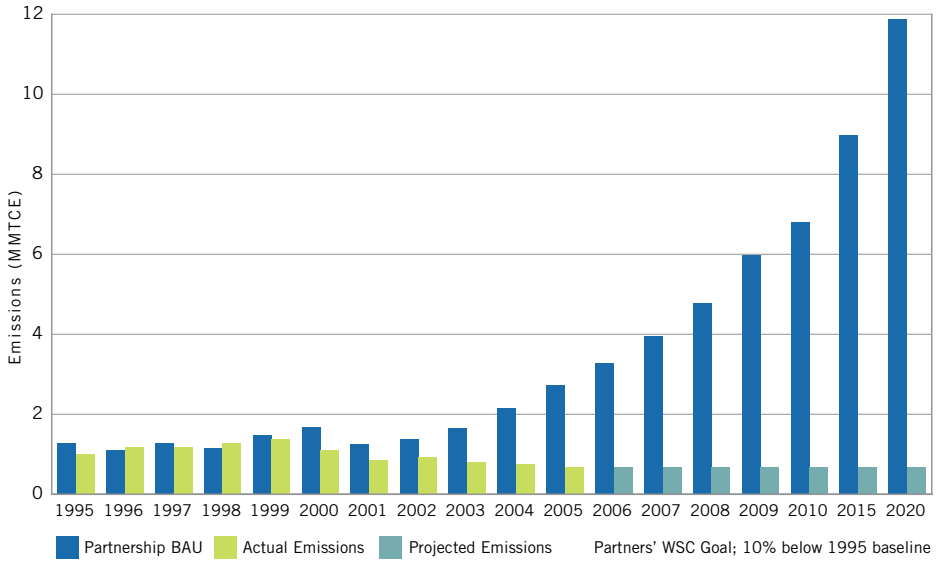


Figure 4 – Actual and expected WSC emissions



The emission trends of partners participating to WSC PFC agreements are reported in figure 4[10] in comparison with a business as usual (BAU) scenario blue columns. This demonstrates the commitment of the semiconductor industry to reducing PFC emissions.

The European semiconductor industry – although being a minor contributor to overall emissions and in spite of the high costs associated with emission reduction in the sector – accepts full responsibility to make its contribution to reduce global warming by voluntarily reducing its PFC gases emissions.

7. Conclusions

The European semiconductor industry – although being a minor contributor to overall emissions and in spite of the high costs associated with emission reduction in the sector – accepts full responsibility to make its contribution to reduce global warming by voluntarily reducing its PFC gases emissions. As the first industry to coordinate globally and establish a voluntary greenhouse gas emissions reduction goal, the semiconductor industry has established itself as a leader and model for other industrial sectors. The industry has been recognised in Europe and the US for its proactive approach.

The semiconductor industry 10% reduction goal will be reached in 2010, despite a significant increase in wafer demand over time. A focus on aggressively reducing C_2F_6 emissions will lead the European industry to achieving or even surpassing the 10% goal. If the current normalized PFC emissions trend continues and wafer demand projections are accurate, the European industry will achieve the 2010 goal. However, the industry must closely monitor the "ramping up" of lower emitting advanced 200mm and 300mm fabs and the performance of older fabs to ensure they proceed as anticipated. Some emerging technologies and processes will represent new application for PFC gases and must be carefully monitored. If a significant number of older technology fabs continue operations beyond 2009, aggressive measures will be required to reduce PFC emissions from those fabs.

10 Scott Bartos US EPA, *ISESH 06 Conference*, Malta June 2006

EECA-ESIA

The European Semiconductor Industry Association (ESIA), part of the European Electronic Component manufacturers' Association (EECA), represents the European-based manufacturers of semiconductor devices. The semiconductor industry provides key enabling technologies at the forefront of the development of the digital economy. The membership supports over 100,000 direct jobs in a consumption market valued at around €31.8bn in 2006.

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