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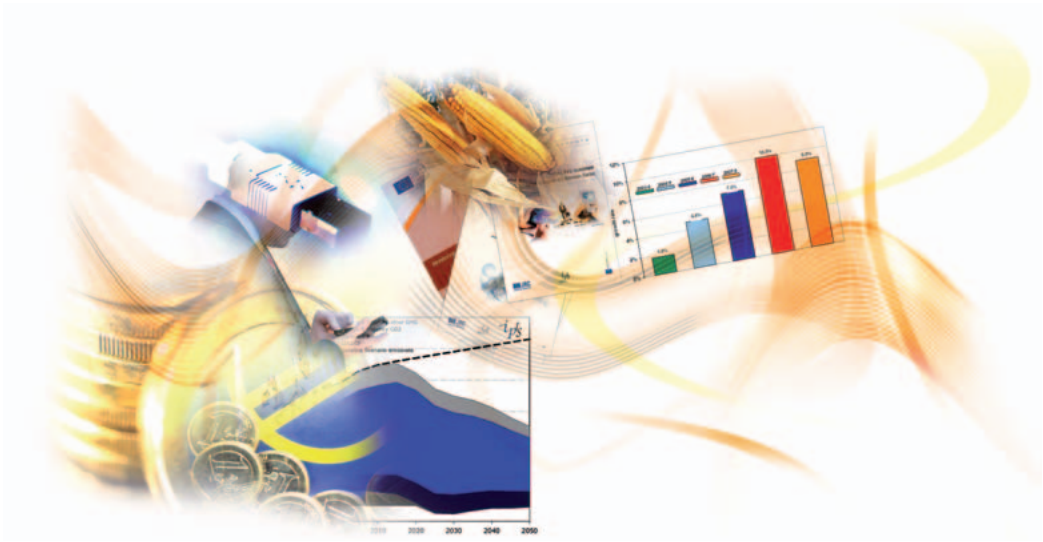
The Future of Semiconductor Intellectual Property Architectural Blocks in Europe

Author: Ilkka Tuomi
Editor: Marc Bogdanowicz



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The mission of the JRC-IPTS is to provide customer-driven support to the EU policy-making process by developing science-based responses to policy challenges that have both a socio-economic as well as a scientific/technological dimension.

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Preface

Over the last decades, developed economies have been undergoing a structural transformation towards knowledge economies. Trends include:

- A growing and now dominant share of the economy represented by "services",
- Extended and sustained growth of knowledge assets with supporting changes in R&D activities, education, lifelong learning, etc,
- A shift in the economic activity of developed economies to concentrate on the higher levels of the value chain. Manufacturing diminishes as a percentage of total output, often moving rapidly to lower-cost locations (mainly Asia).

Throughout the brief 50 year history of the semiconductor industry, its innovation and growth have been fuelled by rapid technical evolution. This has led to changes in the structure of the industry that have many similarities with those in the wider economy. In particular, the ownership and trading of intellectual property and the respective innovative business models have not only been hot topics of discussion at conferences and workshops but have also led to the creation of new industry segments. Over the past two decades, structural changes in the semiconductor "value chain" have led to the emergence of businesses dedicated to the development of computing cores which have rapidly proliferated into a very diverse range of consumer products.

Indeed, I was employed as a designer in the IC industry 30 years ago and was responsible for the development of one of the first commercially available CMOS cell libraries. Although this was a rudimentary predecessor of the IP cores and function blocks available today, many of the technical and commercial questions remain, albeit with many magnitude changes in complexity. Trade-offs between development time and costs, and between custom-dedicated and programmable must be weighed up. Factors such as optimisation of chip size, yield, cost, maximizing function, minimizing power consumption vs. redundancy, flexibility and programmability must also be carefully considered at the conception of a new product design and debates are even more complex and intense today than they were one or two decades ago.

IP-centric, fab-less companies are essential actors in the value chain. Hardware commoditisation has converted architectural IP and software into the main differentiation factors, and IP-centred companies into essential actors in the semiconductor industry value chain. The progressive relocation (to Asia) of the foundry companies, and consequently that of IP-centred activities close to their test sites (“*the fab is the lab*”) and also close to their markets (corporate manufacturing sector users: automotive, telco equipment, etc.), questions the very viability of European IP-centred companies and, in more general terms, the move to the higher levels of the value chain. The projected end of semiconductor scaling is posing additional vital challenges to the whole sector.

This report reflects the findings of the study, carried out by JRC-IPTS at the request of DG Information Society and Media, on the IP-centred industry. The report offers insights into the intellectual property business, and discusses the changing role of “drivers”, including the emergence of Asian actors and the

potential impact that may result as we approach limits in terms of technology scaling. It concludes by discussing the competitiveness of the European IP-centred industry and the policy-related issues that may impact future competence development, access to design tools, relevance of roadmap activities, intellectual property legislation, and emerging innovation models.

David Broster
Head of the Information Society Unit
JRC IPTS

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1. Executive Summary

During 2008 and 2009, the Information Society Unit of the Institute for Prospective Technological Studies[1] ran a research project on semiconductor intellectual property (IP) blocks, also known as IP cores. This project was launched at the request of the Directorate General Information Society and Media of the European Commission, and the research was conducted by Oy Meaning Processing Ltd. The study collects and analyses data on IP blocks, with a special focus on the future competitiveness of the related European industry.

Semiconductor intellectual property (IP) blocks, also known as IP cores, are reusable design components that are used to build advanced integrated circuits (ICs). It is typically impossible to create new IC designs without pre-designed IP blocks as a starting point. These design components are called "intellectual property" blocks because they are traded as rights to use and copy the design. Firms that focus on this business model are often called "chipless" semiconductor firms.

IP cores are perhaps the most knowledge-intensive link in the information economy value chain. They define the capabilities of billions of electronic devices produced every year. As all products are becoming increasingly intelligent and embedded with information processing and communication capabilities, future developments in semiconductor IP will have a profound impact on the future developments in the overall knowledge economy and society.

At present, the IC industry is approaching the most fundamental technological disruption in its history. The rapid incremental innovation that has led to exponential growth in the number of transistors on a chip and expanded the applications of ICT to all areas of human life is about to end. This discontinuity –the end of semiconductor scaling– opens up new business opportunities and shifts the focus of ICT research to new areas.

The main objective of this study is to describe the current state and potential future developments in semiconductor IP, and to relate the outcomes of the study to policy-related discussions relevant to the EU and its Member States.

Key results of the study include the following:

There are over 150 European firms that license semiconductor IP. Globally, among the top 20 independent IP vendors, nine have headquarters in the EU or have substantial development activities in European countries. At present, many IP vendors have difficulties with profitability and growth. The approaching technology disruption will, however, create new business models and potentially lead to rapid expansion of innovative activities in semiconductor-based industries.

Asian countries are implementing focused policies that aim to create and support semiconductor ecosystems that span from design to final system production. China –the largest semiconductor consumer worldwide– is still catching up technology leaders both in design and chip fabrication. The slowing down of advances in IC fabrication technology will, however, make this lag increasingly unimportant. There are now about 500 semiconductor design enterprises

1 The Institute for Prospective Technological Studies is one of the seven research Institutes of the European Commission's Joint Research Centre.

in China, although only a handful are actively marketing their IP outside China. China may be relatively well positioned for the new business logic and IP architectures that emerge at the end of semiconductor scaling in the next years.

Product reconfigurability is also becoming increasingly important in semiconductor hardware. Reconfigurability means that processing architecture can be changed according to the needs of the computational problem at hand. This will change the traditional division of labour between software and hardware, and make high-performance computation possible with relatively low-performance processing technologies.

When reconfigurable application-specific hardware architectures are combined with low cost implementation technologies, radically new domains of innovation become possible in the ICT industry. New downstream innovation models will become important. The realisation of emerging opportunities will, however, critically depend on wide access to design tools and competences. To a significant extent, the future of semiconductor IP depends on competence development that occurs in open innovation ecosystems and outside formal educational settings.

Several entry barriers limit growth in this area. Research policies that encourage the development of open design ecosystems, low-cost design-to-implementation paths, new forms of competence development, and new computational models could have high impact on the future of IP architectures in Europe. As the IP industry and its knowledge processes are based on global networks, regional policies have to be formulated in a global context, for example, as policies that facilitate the formation of strategic ecosystem hot-spots. In Chapter 9, the report suggests several concrete initiatives that could support policymaking and accelerate growth in this domain.

2. Introduction

2.1. Study Theme and Motivation

This study describes the current state and future development scenarios for pre-designed semiconductor intellectual property cores (IP cores). IP cores, also known as IP blocks and "virtual components," are designs that can be used to build integrated semiconductor devices and "systems-on-chip." They are widely marketed by European, American and Asian firms, and they are critically important building blocks in current and future digital products. Firms can re-use internally developed IP cores in their own products or they can gain revenues through licensing, royalties, and customisation of these pre-designed components. There are over 150 European firms that sell licences to their IP cores. At present, the globally leading vendor is the ARM Holdings plc, based in the UK, whose IP cores were used in about every fourth programmable electronic device manufactured in 2007.

As technology allows now billions of transistors on one semiconductor die, it is impossible to build new chips from scratch. Instead, designers start with large libraries of semiconductor IP and construct new chips by combining, modifying, and complementing earlier designs. Often dozens or more IP blocks are combined in one chip to create Application Specific Integrated Circuits (ASICs), Application Specific Standard Products (ASSPs), and complete Systems-on-Chip (SoCs). These, in turn, provide the foundation for products such as mobile phones, television desktop boxes, digital cameras, MP3 players, automobile engine and industrial process controllers, toys, smart cards, hearing aids, heart monitors, and basically everything that uses or processes information and data.

As the design of IP cores often requires expertise both in microelectronics design and demanding application domains, specialised firms that develop IP cores represent a highly knowledge-intensive segment of the ICT industry. IP cores are used in almost all new semiconductor chip designs, and they are critically important for the successful introduction of new electronics products. The future of this industry segment is therefore of major importance to the European information economy.

In the history of the semiconductor industry, manufacturing, assembly and testing activities have relatively rapidly moved to countries with low manufacturing costs. Today, with the exception of Intel, IBM, Samsung and few other Integrated Device Manufacturers (IDMs), the actual manufacture of semiconductor chips is dominated by firms located in Taiwan, China, and Singapore.[2] Also Intel and IBM are increasingly producing leading-edge semiconductors in Asia. Intel started the construction of its first semiconductor manufacturing plant in China at the end of 2007, investing $2.5 billion in the project. In December 2007, IBM, in turn, licensed its advanced 45 nanometre technology to SMIC, now globally the third-largest independent semiconductor manufacturer, based in China. The present study, therefore, also discusses the current and potential geographic relocation of design activities of semiconductor IP cores, and its possible policy implications.

The semiconductor industry is today in a historically unique situation. For almost five decades the industry has been driven by

2 In 2007, the Taiwanese TSMC and UMC, the Chinese SMIC, and the Singaporean Chartered Semiconductor were the leading independent semiconductor foundries, with a market share of 71 per cent.

continuous miniaturisation. The size of transistors on semiconductor die is now measured in nanometres. The smallest features on leading-edge chips are now down to three atomic layers. As the cost of manufacturing has remained almost constant per square millimetre, transistors are now tens of millions times less expensive than they were just three decades ago.

This improvement is a key factor in the emergence of the information economy and knowledge society. The predictability and constancy of improvements in the semiconductor industry has defined business logic in the industry and also widely beyond it. Many industries now explicitly or implicitly rely on continuous technical progress in the semiconductor industry. In the near future, this fundamental driving force will evaporate. Miniaturisation is becoming increasingly expensive, its technical and economic benefits are declining, and new alternative sources of value are emerging in the knowledge economy.

This technical discontinuity will have huge implications. It will show up in macroeconomic indicators of productivity and growth, and it will make us ask why, exactly, smaller transistors were considered to be better. At the same time, new business models will emerge, and new sources of value will be defined and appropriated. Value added in design is becoming increasingly important as incremental technical improvement slows down. The present study claims that to understand the emerging opportunities, we need to understand the "chipless" model, which focuses on creating re-usable intellectual property blocks and processing architectures.

Semiconductor IP represents a very knowledge-intensive part of the ICT industry, and one of its highest value-adding activities. Basically, it packages and resells pure knowledge. Changes in the semiconductor IP sector, therefore, are potentially important for the USD 1.5 trillion electronics industry, as well as for the rest of the knowledge economy.

2.1.1. European Intellectual Property Architectures in the Global Context

Europe is today a relatively strong player in the semiconductor IP field. Although European and global semiconductor firms now manufacture many of their products in Asia, Europe has several leading IP firms and over 150 small IP vendor firms. The semiconductor wafer manufacture is now dominated by dedicated Taiwanese, Chinese and Singaporean firms, and also large IDMs now increasingly outsource wafer production to Asia. The leading edge general-purpose microprocessor production, in turn, is led by traditional integrated device manufacturers such as Intel, AMD, and IBM. Although semiconductor design is increasingly done in countries such as India, Europe still has strong capabilities in IP creation, and good possibilities to stay at the leading-edge in the semiconductor IP industry. European researchers have also developed new innovative processing architectures, and several semiconductor IP start-ups have been launched in the EU as a result of university research.

In geographical terms, the UK is the leading EU country in semiconductor IP, though successful IP firms exist in most EU countries. We describe the European IP vendors in more detail in subsequent chapters of this report. We also highlight some of the factors that have led to geographic concentration of semiconductor design activities on the global and European levels.

Although this study estimates that the revenues generated by the chipless semiconductor firms are less than one percent of the total semiconductor industry, it is important to understand the reality behind the numbers.

First, the semiconductor IP industry creates inputs for the semiconductor industry. It is

therefore not possible to estimate the economic impact of semiconductor IP simply by comparing these two industries using their revenues. In fact, the size of the IP market should be compared with the semiconductor design services market. The semiconductor IP industry is essentially about semiconductor designs that are sold as pre-packaged products. Often the package comes with consulting and customisation. At one extreme, the design work is done to the specifications of a customer. In that case, market analysts categorize the activity as design service. When the design is sold as a licence to use and copy a design component, the activity is categorised as IP.

Gartner Inc. estimates that the global semiconductor design services revenue in 2008 was about USD 1.7 billion. This is almost exactly the size of the chipless semiconductor market. In other words, about half of the semiconductor design market consists of design services and about half pre-designed IP blocks. As IC design houses also extensively reuse their internally developed IP blocks, the exact proportions of revenues are, however, quite impossible to estimate accurately.

Second, the majority of commercially used semiconductor IP is not visible. For example, Semico estimates that about four or five times more reusable IP blocks are developed internally than are sold on the market. The volume of reusable IP design activities, therefore, may well be five times bigger than market studies estimate. As the processes for managing and packaging IP blocks mature inside semiconductor firms and as it becomes increasingly necessary to create reusable IP as the complexity of designs increase, this internally developed IP can relatively easily be used to create additional revenues. Potentially, the visible IP market could rapidly increase as such internal IP would enter the market.

In general, IP creation is among the highest value adding activities in the ICT production, and its economic impact is often grossly underestimated. The semiconductor IP segment, therefore, represents interesting policy and business opportunities, as the ICT industry enters a period of technical disruption in the next years.

2.2. Scope of the Study

In the present study we define intellectual property cores as pre-designed components that can be combined with other design elements to form a functional system. Traditionally, IP cores have been implemented on semiconductor die, either in Application Specific Integrated Circuits (ASICs), or on Field-Programmable Gate Arrays (FPGAs).[3] Emerging technologies, such as printed organic electronics, however, can potentially also be used to implement IP cores in the future. Although the focus of the study is on semiconductor IP cores, it also takes into account developments occurring beyond the present semiconductor industry.

New technologies, including carbon nanotubes, graphene transistors, self-organising molecular devices, and quantum computing can potentially bypass the physical limits of known semiconductor technologies. Eventually, such radical new technologies could substitute current technologies and enable progress in ICTs. The present study does not discuss these future technologies in any detail, for a very simple but important reason: it starts from the observation that even if radical new technologies were available today in industrial volumes, their deployment would require knowledge, manufacturing technologies, and design methods and tools that are radically different from those currently used in the semiconductor industry. The underlying claim is a rather strong one. Even if, for example, new carbon-based transistors and full-scale manufacturing methods for them existed today, the industry would still face a

3 The appendix describes ASIC and FPGA design processes in more detail.

major technical disruption that would rewrite the rules under which it has operated for the last several decades. This disruption will occur irrespective of whether the new technologies are there today, or in thirty years time. Although the full story is obviously more complicated, the present study empirically focuses on the current industrial reality and simultaneously argues that the continuous progress that characterised the development of ICTs is about to end. The analysis of future developments in the semiconductor IP industry is therefore based on charting the current business landscape and generic patterns of technology development, instead of focusing on possible scientific breakthroughs and innovative new technologies. A further justification for this approach is that there are no known alternatives for the currently used technologies that could be manufactured in industrial volumes in the foreseeable future.

The specific empirical focus of the present study is on IP cores that can be programmed and combined into larger processing architectures. The study defines such IP cores as *IP computing cores*. These are, typically, programmable microprocessors, micro-controllers, digital signal processors, analog-digital mixed-signal processing blocks, and configurable computing architectures. As computing cores typically require additional IP components to create a fully functional chip or a system-on-chip, these complementary components are also taken into account when relevant.

For the purposes of the present study, it is not necessary to categorise different types of semiconductor IP in any great systematical detail, although it is useful to understand that different economic constraints and innovation dynamics underlie different IP product segments. In practice, market analysts often distinguish many different types of IP to segment the market and to cluster vendors. Such segmentation is not trivial, and methodological differences sometimes lead to widely varying estimates of IP markets. In practice, IP is packaged in many ways, vendors continuously develop their business models, and entries, exits and mergers change the business landscape so fast that data is barely comparable across the years.

Market studies sometimes differentiate between two types of semiconductor intellectual property: design IP and technology licensing. Technology licensing is used to transfer rights to use patented inventions. Design IP, in turn, consists of documented designs that the licensor can use as components in the licensor's own designs. According to preliminary data from Gartner Inc., the global semiconductor design IP market was USD 1.486 billion in 2008, whereas semiconductor IP technology licensing was worth USD 586 million.[4] The various semiconductor IP categories used by Gartner are shown in Table 1.

In the present study, we use a wide variety of market studies, industry reports, business news, and primary data collected on IP firms and their activities. We have also conducted several case studies that focused on the histories and growth patterns of selected IP firms. Going beyond a simple description of the current state of the IP segment, we also interpret the current situation and future developments in the broader contexts of globalisation and technology and innovation studies.

In the next chapter, we discuss major socio-economic trends, as economies, products, and organisations enter the new knowledge-based era. We focus on the challenges of traditional intellectual property, new innovation models, and policy. Semiconductor "intellectual property" is often a misleading term, as it tends to put the semiconductor design segment into a context

4 The data is a preliminary estimate for 2008. One should also note that the numbers do not add up. The total volume of the various IP segments in the table is USD 1,540 million. Assuming that technology licensing is counted as a separate IP category, the total market would be 2,127 million.

Table 1: Semiconductor IP in 2008, as categorised by Gartner Inc.

		USD millions	Growth %
Processors	Microprocessors	582	6.2
	Digital Signal Processors	52	21
Physical IP	Analog and Mixed Signal	205	22.4
	PHY	149	8.4
	Memory cells/blocks	132	4
	Physical library	62	-6
Other IP	Fixed function signal processing	182	16
	Interface controllers	79	5.5
	Block libraries	29	-16.5
	Infrastructure IP	34	3.1
	Miscellaneous IP	28	-11.4
	Controllers and peripherals	6	-15.2
	Total design IP	*1486*	*8*
	Technology licensing	587	6.8
	Total IP	**2073**	**7.7**

where the concept of intellectual property and intellectual property rights would be central. This is rarely the case in practice, as can be seen during the following chapters. Yet, the semiconductor IP segment is characterised by the fact that it trades intangible assets, and the structures of intellectual rights regimes are important for its future. We highlight some key issues, and provide some references for further discussions. Similarly, we briefly revisit some key themes of recent innovation research, as they inform and underlie various sections of the report, including its policy proposals. The chapter also discusses the possibility that the wide use of ICTs has actually changed the fundamental conditions for making policy. We frame this discussion in the context of long waves of economic growth and the impact of key technologies, showing how developments in the semiconductor technology potentially destroy the historical patterns of growth and crisis, also known as the Kondratieff waves. The aim of the chapter is to give some perspective to the rest of the study and to help the reader think about changes that occur outside the semiconductor industry that could shape its future in important ways.

Chapter 4 switches from this conceptual discussion to a more data-oriented approach. It describes the current reality of the semiconductor industry, describing its business models and value creation activities both in qualitative and quantitative terms. We then focus on the semiconductor IP industry itself, providing data on the IP market and supply, including geographic patterns of production. To get a better understanding of what typical IP firms actually do, we provide a detailed description of Swedish IP firms and a brief outline of the historical development of the largest IP vendor, ARM Ltd.

Chapter 5 describes in details the IP market, its suppliers and consumers. It gives comparative data for different geographical regions and offers a more in-depth view of the Swedish IP vendors as well as of ARM Holdings, the worldwide leading company whose headquarters are based in UK.

Chapter 6 moves to the main historical drivers in the semiconductor industry, first focusing on the continuous miniaturisation and its impacts, and then discussing economic trends and patterns of internationalisation. In discussing the historical development of internationalisation, we highlight the factors that underlie the prominence of Silicon Valley and East Asia as global hubs in semiconductor production.

Based on innovation and technology studies, we then try in the following Chapter 7 to uncover major drivers that could shape the future of semiconductor IP and information processing architectures. The chapter is obviously speculative in nature, as we talk about generic trends that cannot be verified at this point in time. Specifically, we discuss the future of Makimoto Waves that have been claimed to drive the industry through cycles of standardisation and customisation. We also propose a new model that links reconfigurable IP architectures to user-centric innovation models.

One question of intrinsic interest to regional policymakers is the potential of China as a semiconductor IP creator. In the history of semiconductors, production tasks and segments of value chains have rapidly moved to East Asia and, more recently, to China. We describe in Chapter 8 the status of the IC design segment in China, highlight some recent policy issues, and evaluate five possible trajectories that could make China a prominent IP actor.

Finally, in its last chapter, the report suggests several policy implications. We present a generic model of entry and exit in the IP segment, and use it to highlight key areas where policy could make a difference. These include new approaches for competence development, expanded access to design tools in open development ecosystems, and new low-cost realisation paths for designs and experimentation. We further highlight the need for new computational models, including reconfigurable hardware processing architectures, and suggest that latent opportunities could be made visible and explicit by a new type of roadmap activity organised around small IP vendors and developers. We also point out some potentially important areas for policy-related research. These include new approaches for regional policies that facilitate the growth of local hot-spots in global innovation ecosystems, and research on the enablers of the open source development model in the hardware domain. The latter we consider important, as the open source model has shown its potential to lead to very fast growth in the software domain, as well as its capability to reorganise existing industries and business logic.

3. Emerging Discontinuities

In the next years, the semiconductor industry is about to experience a major discontinuity, with vast economic and social ramifications: The end of scaling of the physical dimensions of components on integrated circuits. When Jack Kilby created the first integrated circuit in 1958, it contained two transistors and a couple of other components.[5] Today it is easily possible to package tens of millions of transistors on a chip of same size. For fifty years, engineers have found ways to print smaller and smaller features on silicon wafers. As chapter 2 describes in more detail, in the second half of 1990s, when the developments in optical lithography were exceptionally fast, the physical dimensions of the smallest component features declined 30 percent every two years. This implied halving of the component area requirements in about the same time.

In high-volume semiconductor components, such as microprocessors and memory chips, this technical advance has been translated into rapidly declining component costs. In the second half of the 1990s, the cost of a transistor on a microprocessor chip declined 60 percent, annually. This was exceptionally fast, but typically the declines of quality adjusted prices have been over 40 percent on annual basis.

We can imagine an economic crisis, where the stock market value drops 50 percent in a year, resembling what we saw in 2008. Then we have to imagine that this crisis continues without abatement, 35 years. That gives a rough scale of the change that has occurred in the semiconductor processor industry.

The end of semiconductor scaling will therefore be a major technical disruption. It will also occur at a time when it is possible to package more transistors on a chip than most applications need, and also more than designers are able to effectively use. As Bass and Christensen noted some years ago:

"This is precisely the juncture at which the microprocessor market has now arrived. Price and performance, fuelled by the industry's collective preoccupation with Moore's Law, are still the metrics valued in essentially all tiers of the market today. Even so, there are signs that a seismic shift is occurring. The initial, performance-dominated phase is giving way to a new era in which other factors, such as customization, matter more."[6]

Although commentators of the industry tend to highlight bleeding-edge advances in the industry, the real action is often elsewhere. Strictly speaking, the most advanced semiconductor technologies are used for niche products. Although the cost of transistors has radically declined during the last six decades, a low-cost transistor on a bleeding edge semiconductor chip now costs over 50 million USD to create. Basic economics means that these chips can only be used for products that can be sold in tens of millions of copies. It may be odd to call these products niche products, as hundreds of millions of consumers use PCs, DVDs, digital set-top boxes, MP3 players, digital cameras, and mobile phones.[7] In practice, however, bleeding edge technologies are used only in a small number

5 Kilby's patent application, filed in February 1959, shows two transistors, eight resistors, and two capacitors. Robert Noyce, from Fairchild Semiconductor, filed a patent in July the same year, with one transistor, two diodes, three resistors, and two capacitors. The Noyce patent became the foundation of the planar process of making integrated circuits.

6 Bass & Christensen (2002, 35).

7 According to estimates from Gartner, Inc., in 2007 the top ten original equipment manufacturers accounted for USD 91 billion of semiconductor consumption, or about a third of the total. The biggest semiconductor users were Hewlett-Packard and Nokia. Today, about two-thirds of semiconductors are used for PCs and mobile phones.

of high-volume products, and very many digital products are built using technologies that were new ten or twenty years ago. The most technically amazing advances in semiconductor technology, therefore, tend to be irrelevant for many potential users of information technology. More importantly, great potential for future innovations in ICTs can be found from this "long tail" of semiconductor technology, as discussed in Chapter 6.

Christensen, quoted above, is known for his research on disruptive technological change in the computer industry. According to Christensen, the leading firms tend to fail and new entrants usually become industry leaders when the underlying technology does not improve incrementally.[8] A recurring pattern in many technology-based industries, including mainframe, PC, and automobile production, has been that the source of competitive advantages moves from performance to reliability, then to convenience and finally to customization. When performance starts to exceed user requirements, the market becomes segmented into tiers, where only few customers are focusing on high performance at any cost. Most customers are willing to trade off cost and performance. Further, the product characteristics that customers were willing to pay for shift from leading-edge performance to reliability, convenience and customization. Bass and Christensen conclude that:

"The fact that microprocessor designers are now 'wasting' transistors is one indication that the industry is about to re-enact what happened in other technology-based industries, namely, the rise of customization. ...Modular designs by definition force performance compromises and a backing away from the bleeding edge."[9]

On a more macroeconomic scale, the discontinuity created by the end of scaling will match the neo-Schumpeterian interpretations of long waves in economic growth and productivity. The end of scaling, therefore, could be interpreted as the end of the most recent Kondratieff wave.[10] Below we argue, however, that advances in the semiconductor industry have been profound enough to break the historical patterns that created the Kondratieff waves, making semiconductor IP an especially interesting opportunity for future growth.

3.1. The New Paradigm of Knowledge Economy

The present study focuses on intellectual property -based business models in the semiconductor industry. IP-based businesses rely on copyrights and patents, as they need to publish specifications of their knowledge-based products. The actual licensing agreements are made between known parties, and can therefore be completed as normal business contracts. Intellectual property rights, however, are important for protecting created knowledge and products against unauthorized copying and use. Technical and legal protections for IP are therefore actively developed and promoted by semiconductor industry firms and associations. Until recently, many semiconductor firms have, for example, been reluctant to locate design activities in China due to the perceived lack of IPR enforcement and protection.

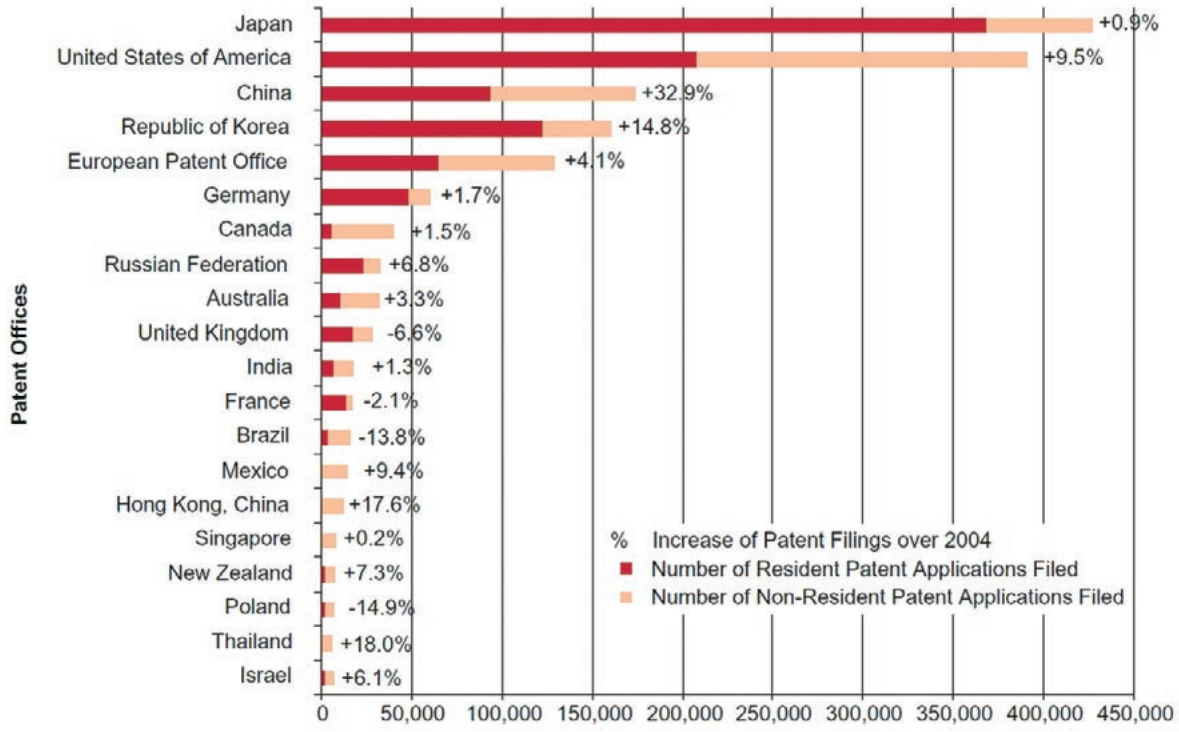
The protection of outputs of the IP industry is an important issue for IP vendors. More fundamentally, however, the IP-based industry is a knowledge-based industry, where the critical inputs are intellectual assets. It is fundamentally an industry driven by innovation. To understand the IP-based business models and their economic impact, we, therefore, have to adopt a broad view

8 Cf., Bower & Christensen (1995), Rosenbloom & Christensen (1994), and Christensen (1997).

9 Bass and Christensen (2002).

10 Kondratieff waves in economic development have usually been described as large-scale fluctuations in global economic growth patterns that last about 40 to 60 years. For references and discussion, see section 3.3.

Figure 1: Resident and non-resident patent applications in different countries, 2005



Source: WIPO, 2007

on intellectual assets generated in the industry. Some of these are traditional intellectual property assets; the role of traditional IPR, however, is also becoming less visible as design firms focus on continuous rapid innovation and the development of innovation ecosystems.

Today, intellectual assets are still rarely included in national and business accounts.[11] Typically, investments in knowledge are interpreted as final or intermediate consumption. Preliminary estimates in countries such as Finland, Japan, the U.K., the Netherlands, and the US put the annual investments in intellectual assets at around ten percent of GDP.[12] In the US, the investments in intangible assets exceeded the investments in tangible assets in the 1990s, and in the late 1990s, the US non-farm output was underestimated by about 1 trillion USD and the business capital stock by 3.6 trillion USD due to the invisibility of investments in intellectual assets.[13]

The estimated size of the knowledge-based economy is now rapidly growing, both because knowledge is becoming visible in the national and organizational accounting systems but also because business success is becoming increasingly dependent on knowledge and innovation. One indication of this is the increasing patenting activity around the world. According to the 2007 Edition of the WIPO Patent Report there

11 Intellectual assets are often defined to include investments in research and development, patents, software, human skills, and structural and relational capital in organizations.

12 Cf. OECD (2008a).

13 Corrado, Hulten, Sichel (2005; 2006). Corrado *et al.* estimate that "bricks and mortar" investments accounted for less than 8 percent of total output growth per hour in the period 1995-2003 in the US. Corrado *et al.* Categorize intellectual asset investments into three major groups: computerized information, innovative property (R&D and design), and economic competences that include brand equity, firm-specific human capital and organizational capital. All these forms of assets clearly depend on ICTs.

were approximately 5.6 million patents in force worldwide at the end of 2005, and more than 1,6 million applications were filed in the same year. As can be seen from the Figure 1, the fastest growth in patent applications was in China.

Whereas patents represent one output of the knowledge economy, research and development is one of its key inputs. In the OECD countries, R&D expenditure climbed to USD 817.8 billion in 2006, up from USD 468.2 billion in 1996. In real terms, R&D spending grew at between 3.2 and 3.4 percent a year from 1996 to 2006. In the present decade, China has rapidly grown its R&D expenditures. In 2006, China's gross domestic expenditure on R&D (GERD) reached USD 86.8 billion, or about one third of EU GERD at the same year.[14]

The concept of intellectual property is not a trivial one, and some sophistication is needed when policies are developed in IP-related domains. Knowledge is not a "thing" that can be possessed and owned as material assets. Knowledge gains and loses value in social and material contexts, and it also reflexively changes those contexts. In general, new knowledge potentially changes the underlying systems of value.[15] Classical economic concepts, therefore, can not in any straightforward way be used to analyze knowledge economy. Knowledge is also an inherently social and relational phenomenon. Knowledge is embedded in culturally meaningful technologies and social practices. The concept of intellectual property, therefore, is in many ways theoretically broken, and it easily misses many characteristics that are important when we try to understand knowledge-based economy.[16] Yet the concept originates from concrete social and economic problems that need to be addressed also today.

The Statute of Anne, which laid down the modern principles of intellectual property rights in 1710, aimed at balancing two conflicting interests: the wide diffusion of new knowledge for the benefit of the society, and the economic interest of the creator of the new knowledge. The Statute solved this problem by granting the creator the monopoly rights for copying books for fourteen years, after which the knowledge was put in the "public domain," where it was freely available for anyone.[17] The Statute noted that frequent copying without the consent of authors or proprietors had lead to their "great detriment, and too often to the ruin of them and their families." On the other hand, the monopoly was limited, as monopolies were considered to be harmful, for example, because they were usually associated with artificially high prices.[18]

The Statute of Anne focused on copyrights. Following its logic, the broader concept of "intellectual rights" was introduced in the U.S. Constitution in 1787.[19] Intellectual rights became known as intellectual property rights as publishers started to argue that authors have "natural rights" to the ownership of their works. Publishers argued that intellectual rights should be perpetual, as they were a form of property.[20] This view was particularly influential in France, where, for example, the Paris Book Guild hired the encyclopaedist Denis Diderot to write a treatise that would promote the Guild's interest in literary rights.[21]

14 Data from (OECD 2008b).
15 Tuomi (1999).
16 For an overview, see, e.g., Jaffe and Lerner (2004).

17 The copyright monopoly could be extended for another fourteen years if the author was still alive when the original copyright period expired.
18 The Statute therefore also included a clause that enabled anyone to make a complaint if the price of the book seemed to be artificially high (Tuomi 2004a).
19 Specifically, the Constitution stated: "the Congress shall have the power…to promote the progress of science and useful arts, by securing for limited times to authors and inventors the exclusive right to their respective writings and discoveries."
20 Ewing (2003).
21 Diderot argued that intellectual property was the highest form of property. He asked: "What form of wealth could belong to a man, if not a work of the mind...if not his own thoughts...the most precious part of himself, that will never perish, that will immortalize him?" (Ewing 2003).

The justifications and the impact of intellectual property laws, therefore, have been debated for long time.[22] In recent years, the debate has again been very active. Many experts now claim that the intellectual property system is seriously flawed. For example, many innovations are system innovations that cumulatively build on earlier innovations and knowledge. When monopoly rights are granted for such incremental system improvements, they tend to constrain future innovation, instead of promoting it. This happens particularly in domains where technology develops fast and product life-cycles are short. Semiconductor IP blocks are often used in such system settings, and IPR regimes can therefore have strong influence on patterns of technology development in this domain. The intellectual property system is also widely used against its original intent. For example, the US patent system allows applicants to postpone the issue of a patent and keep it secret until someone else builds a business on the same idea. Such "submarine" patents have frequently been used to create extraordinary returns also in the semiconductor industry.[23] The innovative quality of granted patents is frequently questioned, in particular in domains such as software development, where innovation is typically based on relatively straightforward engineering work and where prior art has not been systematically archived. In such environments, patents often act mainly as barriers for competition. This is a major problem for small firms and innovators who are not able to use their existing patent portfolios for cross-licensing.[24]

Although it is difficult to revise existing intellectual property regulation, business firms are now actively experimenting with models that could overcome some of the problems in the current IPR regimes. For example, many firms are now trying to use open innovation models.[25] The underlying logic is based on the idea that modern ICT makes it possible to create large innovation ecosystems where value is created by continuous and rapid innovation. As the global innovation system is now producing innovations at high rates, the value of intellectual property monopolies tends to decrease, and in many industries the competitive edge can only be created by innovating faster than the competitors. For many technologies, such as software, the time of securing patent monopoly often exceeds the product lifetime, thus making the benefits from patents questionable. Furthermore, as the enforcement of patent rights tends to be very expensive and difficult, many firms now experiment with business models where intellectual property is not monopolized. For example, Sun Microsystems now licenses the designs of its SPARC microprocessors using an open source license. In the software domain, this open source approach, of course, has been widely used, and, for example, both Google and Nokia license their mobile phone operating systems as open source software.

22 See, e.g., Machlup and Penrose (1950).

23 Graham (2006).

24 Cf. Shapiro (2001), Hall & Ziedonis (2001), Samuelson (2004). For example, Hall and Ziedonis (2001:110) quoted an estimate that a new semiconductor manufacturer should have spent $100 to $200 million of revenues to license what were considered basic manufacturing principles but which did not transfer any currently useful technologies. This, in practice, makes entry impossible for firms who do not have extensive patent portfolios with which they can bargain.

25 The concept of open innovation has been promoted especially by Chesbrough and refined with his colleagues (Chesbrough 2003; Chesbrough, Vanhaverbeke, and West 2006). The key starting point for Chesbrough was corporate R&D, IPR management, and the observation that an increasing amount of knowledge exists and is generated outside the focal firm. In this sense, Chesbrough's open innovation concept aligns with the earlier knowledge management literature that emphasized the importance of intellectual capital (including customer and network capital) as a key productive asset in knowledge-based firms (e.g., Wiig (1993), Sveiby (1997), Edvinsson & Malone (1997), Roos *et al.* (1997), Brooking (1996)). The realization that key knowledge sources exist outside the focal firms also underlies knowledge management and innovation literature that focuses on organizational learning (e.g. Brown & Duguid (1991; 2001)), organizational knowledge creation (e.g. Nonaka & Takeuchi (1995)), and organizational networks (e.g., Powell *et al.* (1996), Hastings (1993)). An alternative model of open innovation is based on user-centric innovation models. We discuss these in the next section.

3.2. Innovation Communities and Ecosystems

The importance of distributed networks has been one of the leading themes in recent innovation research. The traditional view on innovative activity emphasized "heroic innovators," who developed their ingenious insights into new products and services. This model was adapted to organizational product development, which was managed as a fundamentally linear sequence of phases that led from ideas to finished products and their eventual diffusion in the marketplace. More recently, it has been realized that the process is highly iterative and that users are also important sources of product development knowledge.[26] Current research on innovation and product creation has therefore moved toward "open" innovation models that extend the innovation process beyond firm boundaries and "downstream" innovation models, where users actually become the focus of innovation.[27]

In the theoretically strongest interpretation of downstream models, innovations materialize when social practices change and when latent technical opportunities are taken into use in the society.[28] Such downstream models have their roots in empirical research on technology adoption and also theoretical and empirical studies on social learning and knowledge creation. We briefly introduce some key ideas underlying this view, as these new models of innovation have potentially important consequences for both business and policy development.

In strong downstream models, "upstream" innovation is taken for granted. This approach may at first look counter-intuitive and radical. It is, however, supported by many detailed studies of technology development. Upstream innovation, in fact, rarely represents a bottleneck in the innovation process: Instead, reinvention and parallel discovery typically dominate in the upstream, and innovative ideas are often over-abundant. This is not always immediately obvious, as historical retrospection tends to sketch linear paths of progress, often adjusting historical facts to make a story that fits our expectations of how innovation should happen.[29] At the same time, historical accounts obscure the fact that firms and scientists rarely create new ideas. Downstream innovation models are based on the observation that, in practice, the key bottleneck is in the social adoption of latent innovative opportunities.

In the strong downstream models, the users are perceived, not as individualistic consumers, but as members of social communities that maintain specific pools of knowledge and related practices that make new technological opportunities meaningful.[30] In contrast to traditional models of innovation, the focus of innovation, therefore, is perceived to be on the

26 Von Hippel (1988) focused on the role of users as sources of new knowledge and product innovations.

27 This includes von Hippel's recent work, where he has emphasized the importance of distributed innovation models (e.g., Von Hippel 2005; Lakhani and von Hippel 2003; Von Hippel and von Krogh 2003). Along similar lines, a more theoretically grounded model was presented by the current author (Tuomi 2002a), who studied the evolution of Internet-related innovations, including basic networking technologies and the Linux operating system. This downstream innovation model was based on the observation that the focus of innovation can increasingly be found from user communities who actively reinterpret and reinvent the meaning of emerging technological opportunities. Similar emphasis on users as innovators can be found in studies on social construction and domestication of technologies (for a review of these, see Oudshoorn & Pinch (2003)).

28 Tuomi (2002a).

29 For example, official histories of the emergence of packet-switching computer networks and the Internet reorganize events in time and selectively forget facts that do not fit the linear story line (Tuomi 2002a, chap. 9).

30 We contrast here "user-innovator" and "pure" downstream models. In the user-innovator models (e.g. von Hippel), the users contribute new ideas to a quite traditional upstream innovation process. In the pure downstream models, innovation, in contrast, becomes a process of socio-technical change that occurs in social practices. Although "upstream" actors (e.g. business firms) can feed new technical opportunities into the process, innovation can also occur, for example, by reinterpreting and "misusing" existing products. Developments in computer and communication technologies, in fact, have often been driven by unanticipated uses.

innovative and creative activities that occur in the context of use.[31] One important locus of innovation can be found in communities of practice, where social learning and shared interpretations of the world provide the basis for knowledge creation.[32] Upstream and downstream innovators, therefore, are not simply individuals with bright ideas. Instead, innovation occurs in a social structure that consists of a network of specialized communities.[33] An important consequence of this view is that knowledge is not universal, and the world of knowledge is not "flat." ICT reduces barriers created by geographical distance; social boundaries, however, remain highly important for knowledge diffusion and production.[34]

Research on innovation communities has emphasized the fact that innovators rely on social networks and socially mobilized material and cognitive resources. Also cognition, itself, is often distributed among people and technical artefacts. This has important consequences for innovation management in business firms. For example, the downstream view highlights the point that informal social networks that cross organizational boundaries provide the foundation for the creation of new knowledge. Innovation management, therefore, can not be a purely internal affair in business firms; instead, it has to be based on strategic management of knowledge creation and knowledge flows that occur in the broader innovation environment.[35]

When different types of knowledge and expertise are combined and synthesized for new ideas and products, the continuously evolving innovation system can also be viewed as an ecosystem.[36] Such a view on mutual co-evolution of actors can result from a relatively straightforward metaphorical use of ecological concepts. At a more substantial level, it leads to fundamentally social views on technological development. Innovation is not something that happens inside firms. Instead, it is a process where many actors, ideas and technical artefacts co-evolve and provide resources and constraints for change. Most importantly, innovation can not be understood in any simple way as purely technical improvement, as improvement itself can only be understood in a social context that makes the underlying technology meaningful. Although in the industrial society this social context evolved relatively slowly, making it in many cases possible to forget and take for granted the social dimension of technology and innovation, today we live in a world where this rarely is the case.

3.3. Policy at the End of Kondratieff Waves

Innovation has been a somewhat awkward topic for many economists in the recent decades, as the neoclassical theory starts from equilibrium models that are, strictly speaking, incompatible with the idea of innovation. Innovation, therefore, has often been defined in economics as the

31 The underlying theoretical foundations have been discussed in the contexts of knowledge management, innovation theory, and information systems theory by Tuomi (1999; 2002a; 2006).

32 The "community of practice" model was developed in Lave and Wenger (1991), and applied in innovation and organizational learning context first by Brown and Duguid (1991). Nonaka and his colleagues have proposed an alternative model of the loci of innovation, based on the concept of "ba" that was originally developed by the Japanese philosopher Nishida (Nonaka, Toyama, and Hirata 2008). Ba, according to Nonaka *et al.*, provides the shared dynamic context where new meaning and knowledge is created. In contrast to communities of practice, which are based on relatively stable social structures and technology-enabled practices, the concept of ba emphasizes more transient interactions among social participants. The underlying epistemic concepts are rather sophisticated, and have been discussed in detail in Tuomi (2002a; 2006).

33 Brown and Duguid (2000; 2001), Tuomi (2002a).

34 These social boundaries are essentially boundaries of local meaning systems. Social practices and local meaning systems are connected, for example, by boundary objects that are shared across communities of practice (Star and Griesemer 1989), and which include concrete artefacts, design schematics, and, for example, databases (Bowker and Star 1999, chap. 9).

35 In this sense, downstream models share the starting point of "open innovation," as described by Chesbrough (2003).

36 Cf., Moore (1996), and Hagel and Brown (2005).

unexplained component of growth.[37] Research on the economics of innovation, therefore, has often been influenced by socially and historically grounded theories of economy.[38] In recent years, a particularly influential stream of research has formed around studies inspired by the pioneering work of Schumpeter.

A basic question in the Schumpeterian framework is how innovation and technology influence economic growth. Schumpeter's early work focused on long-term economic growth patterns and their links to innovation. This pioneering work has led to a large body of neo-Schumpeterian literature that tries to explain large-scale patterns in the economic history by the underlying changes in key transport, communications, and production technologies.[39]

For example, Perez[40] has highlighted the point that the economic history can be understood as a sequence of techno-economic paradigms, where long-term growth periods have been driven by the wide application of a new general-purpose key technology. According to Perez, the statistically observable long waves of economic growth since the first Industrial Revolution to the emergence of steam power and railways, electrical and heavy engineering, mass production, and, most recently, microelectronics, have been associated with profound changes in the dominant production paradigms. The realization of the economic potential of a new general-purpose key technology requires mutual co-evolution and alignment of social institutions and practices, including legal frameworks, management practices, and industrial relations. Historically, the changes in techno-economic paradigms have been associated with new sources of competitive advantage, new geographical growth patterns, and the decline of old economic centres.

An important outcome of the neo-Schumpeterian analysis lies in its observation that social change is the constraining factor when technological opportunities become transformed into economic value. Technology and the capabilities it affords can efficiently be integrated with social practices only after a gradual process of alignment. As a result, the diffusion of new technologies is strongly constrained by the speed of social and institutional change.[41] Policy, therefore, can also play a crucial role in this change. When new key technologies lead to radical changes in the modes of production, by definition, these changes do not occur easily, and they create conflicts among prevailing interests and powers. This, indeed, can be understood as the fundamental reason why the long waves of economy are long.[42]

The long wave model of economic growth is a controversial issue, and it has been debated for several decades, both on theoretical and empirical grounds.[43] One may, however, ask where are we in the wave of ICT-induced growth? Is the golden age in the future, or is it already in the past?

Indeed, it has been recently argued that we are currently experiencing the end of long waves. For example, Hagel, Brown and Davison argue that:

> "Major technical innovations like the steam engine, electricity, and the telephone brought forth powerful new infrastructures. Inevitably, these disruptive innovations transformed industry and commerce, but

37 Solow's residue, which includes all those sources of productivity growth that cannot be explained, is the most famous example here. Economists have often defined technical progress as the factors that underlie Solow residue.
38 For a discussion of earlier work on innovation and economic theory , see e.g., Rosenberg (1982).
39 See Freeman and Louçã (2001).
40 Perez (1985; 2002).
41 This view, therefore, implicitly adopts the downstream innovation model discussed above.
42 As Kuhn (1970)argued, dominant paradigms often change only after their proponents die.
43 Influential contributions include, for example, (Freeman, Clark, and Soete 1982) and (Kleinknecht 1987). For a discussion on the earlier debates, see Mandel (1995, chap. 6)

> eventually they became stabilizing forces, once businesses learned to harness their capabilities and gained confidence in their new order. That historical pattern –disruption followed by stabilization– has itself been disrupted. A new kind of infrastructure is evolving, built on the sustained exponential pace of performance improvements in computing, storage, and bandwidth. Because the underlying technologies are developing continuously and rapidly, there is no prospect for stabilization."[44]

In other words, if rapid developments in key ICT technologies continue also in the future, it is not obvious that the social institutions, including management practices, ways to organize work, legal frameworks, and geographical focal points of production would be well aligned with the technical opportunities available. The next productivity growth wave, to be created by the wide adoption of ICTs, could simply be destroyed by the same wide adoption of ICTs that also leads to constant reconfiguration of value systems. If social institutions do not "catch up" with the requirements of technology before new key technical opportunities emerge, the social infrastructure does not necessarily have time to stabilize. It has been argued that this, indeed, could be the essence of the "new economy":

> "One of the consequences of the Internet may be that technology development is increasingly unlinked from local social institutions. ... Linux –and other Internet-based innovations– provide examples of socio-technical development that perhaps escape the logic of long waves, and which potentially break long waves into continuous ripples."[45]

The "constant disruption" model of Hagel *et al.* assumes the existence of continuous improvements in computing, storage, and bandwidth. The present study, however, argues that we are about to see a radical disruption in the key technology –integrated circuits– that underlies computing, storage, and bandwidth improvements, and that the rapid continuous improvement in semiconductor technology is about to end. The end result, however, may be the same. A qualitative change has already occurred in the global innovation system, and we do not necessarily need any further developments in the underlying technology to end the long-wave phenomenon. In other words, the basic technological innovations are already there, and the essential components of the knowledge society infrastructure are in place: now the focal areas of innovation move to business models and new applications where the social and cultural dimensions of technology are increasingly visible.

This does not mean that the rate of innovation would slow down. On the contrary, the present study argues that with appropriate policies, new rapidly growing domains of innovation may become available. Although innovation can not be based on semiconductor scaling and its consequences in the future, the basic semiconductor technologies are becoming commodities. The focus of innovation can then move to the uses of the available technological opportunities, also making downstream innovation models increasingly important and visible in practice. This transition may imply new management methods, business models, sources of key knowledge in the semiconductor and ICT industries, and new geographical focal points of economic growth, even when the long-wave model itself would, for the time being, be dead.

The full impact of the new innovation regime obviously extends beyond semiconductor IP industry. It is, however, important to note the possibility that a new innovation regime is emerging where old policy assumptions are not valid anymore. For example, it is possible that technology development is becoming increasingly driven by the fact that market structures and policies can not catch up and become stabilized

44 Hagel Brown, Davison (2008, 82)
45 Tuomi (2002a, 216).

and institutionalized. Under such circumstances new technical functionalities become critical. It is, for example, possible that continuous disruption implies that system reconfigurability is becoming an increasingly important source of value. We return to this possibility in the next chapters.

It is also useful to note that technical developments in semiconductor industry have been a major source of macro-economic productivity growth in recent years. Many influential studies have argued that the production and use of ICTs is a key factor in explaining productivity growth and its differences among countries in recent years. Although it has been rarely pointed out, the rapid development in semiconductors is the main factor that underlies these arguments. In a somewhat simplified way, the measured productivity growth rates have followed the scaling of semiconductors. This is because output volumes have been corrected by price indexes that adjust for the technical improvements of integrated circuits.[46]

Although the present study describes developments in an industry that is conventionally called "intellectual property -based semiconductors," the scope of the study therefore goes beyond traditional intellectual property, such as patents and copyrights. The industry segment that we study could better be called the "intangible semiconductor industry." One could argue that this is the most innovation-intensive part of the semiconductor industry, and the foundation of future information and communication technologies. It is therefore also a good example of the knowledge economy, itself.

46 In practice, the increasing number of transistors on a chip becomes measured as an increase in output volume, even when in purely economic terms output does not grow. As the current-dollar price of new chips at introduction has remained relatively stable over the years, the growth in number of transistors becomes translated into productivity growth. The very fast pace of technical improvements in CMOS technology thus pops-up in macroeconomic studies on growth and productivity. For a detailed discussion, see Tuomi (2004b).

4. The Current Context of the Intellectual Property Architectural Blocks Industry

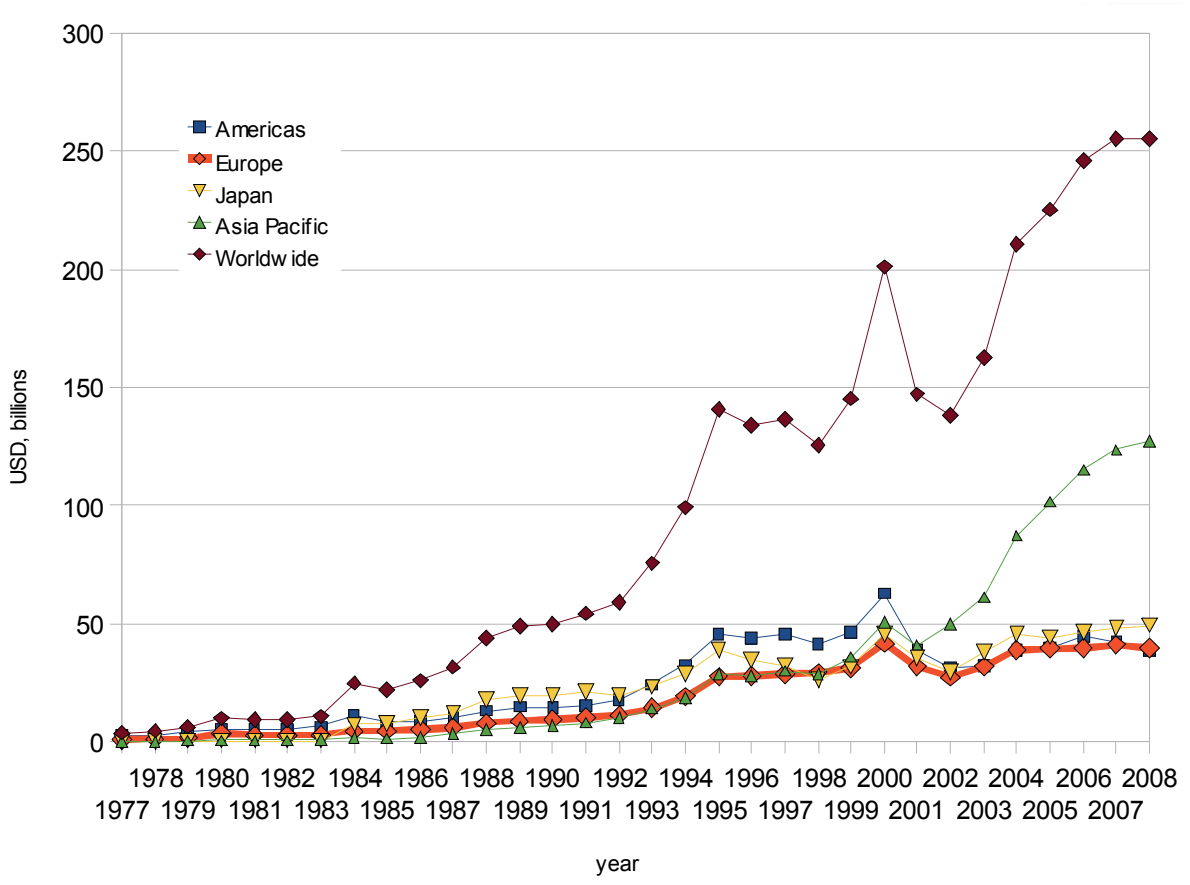
4.1. The Semiconductor Value System

4.1.1. Overview of Semiconductor Consumption and Production

Semiconductors are key components in the roughly 1,400 billion USD electronics industry and provide the foundation for the modern information economy and society. In 2007, the global revenues of the semiconductor industry were about USD 260 billion, according to several market research studies.[47] In November 2008, the World Semiconductor Trade Statistics (WSTS) estimated the global semiconductor market to grow 2.5 percent in 2008 from the previous year, to USD 261.9 billion. Exactly the same revenue

47 Semiconductor Industry Association reported global sales of $255.6 billion, the Global Semiconductor Alliance reported $267.5 billion, Gartner reported $273.9 billion, and iSuppli reported $268.9 billion. SIA reports data from WSTS member organizations, thus giving smaller numbers than, for example, Gartner.

Figure 2: Billings by semiconductor firms in different regions, 1977-2008



Source: calculated from SIA data.

Table 2: Integrated circuit market, 2007-2010, WSTS Autumn 2008 estimate

Billions of USD	2007	2008	2009	2010
Integrated circuits	217,81	220,82	214,66	228,15
Analog	36,45	37,60	35,83	37,81
Micro	56,21	57,08	54,71	57,60
Logic	67,29	77,06	77,38	81,20
Memory	57,85	49,08	46,75	51,54

is expected by Gartner Dataquest, although their estimate actually represents a 4.4 percent decline from 2007. The global downturn has led to a very rapid decline in semiconductor consumption, and in the fourth quarter of 2008 the global semiconductor revenue declined almost one fourth from the previous quarter. The latest estimates by Gartner Dataquest now expect the global revenues to shrink 16.3 percent in 2009, with worldwide revenues reaching USD 219.3 billion.

The largest consumer is Hewlett Packard, which consumed about $15 billion worth of semiconductors in 2007, followed with Nokia, at about $13 billion, and Dell and Samsung, with over $11 billion. Although historically computer manufacturers have been the biggest consumers of semiconductors, in recent years communications and consumer electronics products such as mobile phones, computer games and digital multimedia devices have become the most important growth driver in the industry. In 2007, data processing represented about 37 per cent, communications electronics 28 percent, consumer electronics 18 percent, industrial electronics 9 percent and automotive 8 percent of the total consumption, according to Gartner Dataquest. The top 10 original equipment manufacturers accounted for about a third of all semiconductor consumption.

Since the previous downturn in 2001, the semiconductor market has grown at high rates, with Asia-Pacific leading the growth. This can be seen from Figure 2, which shows the annual bookings of semiconductor firms in the different regions of the world. The annual totals are calculated from the three-month moving averages, as reported by the Semiconductor Industry Association, which somewhat undercounts consumption in China. According to PricewaterhouseCoopers, China used in 2007 more than a third of the ICs developed worldwide.[48]

According to the most recent WSTS estimates, in 2008 the total sales of discrete semiconductors will be USD 17.7 billion, optoelectronics 18 billion, sensors 5.4 billion, and integrated circuits 220.8 billion. The more detailed breakdown forecast for integrated circuits is shown in Table 2.

In 2007, the share of European semiconductor device makers was about 10 percent of the global market. Four European-based firms were among the top 25: STMicroelectronics, Infineon, NXP, and Qimonda. In the first three quarters of 2008, Qimonda dropped 15 positions to number 30, and NXP fell from the 10th position to 15th, according to data from IC Insights. Since then, Qimonda has started insolvency proceedings. In general, mergers, acquisitions, spin-offs, and technology cycles have historically generated large swings in the market size rankings, and market estimates vary somewhat between data providers. In 2008, eight of the top 20 device producers were based in the US, seven in Japan, two in South Korea, and three in Europe.[49] There were no Chinese firms in the top 25 semiconductor device suppliers.

48 Pausa *et al.* (2008).
49 The full list, with headquarter locations, is detailed in Table 4.

4.1.2. Current Business Models

The history of the semiconductor industry has created a complex and rich ecosystem of inter-related actors. Integrated device production started in vertically integrated firms, which since the early 1960s have spun-off specialized industries, including semiconductor equipment manufacturing and silicon wafer production, and since the 1980s, software companies that specialize in electronic design automation tools. Early on, the internal specialization was implemented at a global scale, as was discussed in the previous chapter. Subsequently, this division of labour led to the emergence of specialist firms that now form the globally networked semiconductor production ecosystem.

The core of the semiconductor value system is conventionally understood to be the process that generates semiconductor components for electronic equipment manufacturers. In the next subsections, three different business models are briefly outlined. The first is the traditional integrated device manufacturer (IDM) model, which designs, manufactures, and sells integrated circuits and also discrete semiconductor components. This is the model that historically defines the semiconductor industry. The second business model emerges as a variation of the IDM model: the "fabless" model. It is based on a close cooperation among specialist semiconductor fabrication firms, or foundries, and device producers that operate without their own fabrication plants. The third model is the "chipless" model that focuses on creating and selling designs.

4.1.2.1. The Integrated Device Manufacturer (IDM) Model

The historical evolution of semiconductor industry has proceeded from extensive vertical integration towards specialization and value-chain disintegration.

Up to 1980s, the industry was dominated by independent integrated device manufacturers (IDMs), who relied on their own wafer fabrication facilities and internally developed design tools to make and package integrated circuits. The vertical integration of IDM firms, such as IBM, Motorola, Texas Instruments, and Siemens often extended all the way to electronic equipment manufacturing, using the internally developed chips.

Today, the leading IDM is Intel, with revenues of about USD 38 billion in 2007. Intel provides PC and mobile device chipsets, and networking and memory chips, and it is the leading producer of microprocessors. The research and development costs of Intel were about USD 5.7 billion and the net income about USD 7 billion in 2007. At the end of 2007, it had total assets of USD 55.6 billion, of which property, plant and equipment was USD 17 billion.

4.1.2.2. The Fabless Model

As the industry has been very cyclical, IDMs often have had excess manufacturing capacity that they can sell. Today, most IDMs therefore provide their chip manufacturing or "foundry" capacity to companies that do not have their own fabrication facilities. For example, IBM Microelectronics was the fifth largest provider of foundry services in 2007, with revenues of USD 605 million, according to Gartner.[50] In total, IDM foundry services had about 16 percent of the total wafer manufacturing market in 2007.

At other times, IDMs lack capacity and are willing to buy it. Integrated device manufacturers now therefore also frequently outsource some of their chip manufacturing to pure-play foundries that focus on chip manufacturing. IDMs that extensively use wafer fabrication outsourcing are often described to follow a "fab-lite" business model.

50 According to IC Insights, IBM was the sixth IC foundry in 2007, with sales of USD 570 million. IBMs foundry revenues partly originate from its extensive IP licensing. The actual fabrication is often outsourced. Some commentators, therefore, call IBM a "fabless foundry."

Currently, key IDMs are transforming themselves toward the fabless model. For example, Texas Instruments, one of the largest semiconductor producers, has increasingly used independent foundries. In 2007, it announced that it will stop its internal development at the 45 nanometre process, the current state-of-the-art, and rely on its foundry partners to create chips in the more advanced process nodes. Similarly, AMD announced in October 2008 that it will become a fabless firm and spin off its fabs to a new foundry company that will be majority owned by the Abu Dhabi Advanced Technology Investment Company (ATIC). ATIC has committed up to USD 6 billion to the new firm.

The next section briefly describes the foundry firms that enable the fabless business model in the semiconductor industry.

4.1.2.3. Foundries

A semiconductor foundry is a service organization that processes and manufactures silicon wafers. A typical output of a foundry is a 50-300 mm silicon disk, or wafer, that contains several billions of transistors in a dozen or more layers. A single wafer typically contains several hundred chips, or dies, that are separately packaged when the dies are assembled into a finished and tested integrated circuit product. The foundry business is now dominated by pure-play foundries that do not make their own semiconductor products.

TSMC (Taiwan Semiconductor Manufacturing Company) created the dedicated semiconductor wafer foundry industry in 1987. Although there existed some firms that specialized in the manufacturing of semiconductor wafers already before, the foundry business was a small niche until the end of 1980s. Advances in design tools and the standardization of both design and manufacturing processes have facilitated the transfer of product designs to independent foundries. In the 1990s, the growing markets of telecommunications and multimedia generated increasing aggregate volumes for the new pure-play foundries, accelerating their move down the learning curve. All new semiconductor manufacturers launched after 1990 have been fabless firms that rely on their foundry partners to fabricate their products.

Two Taiwanese pure-play foundries, TSMC and UMC, followed by SMIC in mainland China and the Singapore-based Chartered Semiconductor now dominate the market.[51] The top four now have a market share of about 70 percent of the total foundry market, including foundry services provided by IDMs.[52]

Seven of the top 10 foundries have headquarters in the Asia-Pacific region, two in the US –the merchant IDM foundries of IBM and Texas Instruments– and one in Europe.[53] The European firm, X-Fab, which makes analog and mixed-signal and specialty semiconductors, was the only non-Asian pure-play foundry in the top 14, according to IC Insights data for 2007.[54] As the previously confirmed USD 1 billion incentives in New York were transferred in early 2009 from AMD to the new AMD-ATIC foundry company, now called Globalfoundries, it will become the first pure-play foundry on the American continent. In addition to building a new USD 4.2 billion pure-play facility in Saratoga County, New York, Globalfoundries is also expanding its facilities in Dresden with a new facility towards the end of 2009.

51 Total foundry sales were 22.2 billion USD in 2007 according to Gartner, and 24.5 billion according to IC Insights.

52 Gartner reports 72.7 percent and IC Insights 68 percent.

53 Gartner and IC Insights give different revenues and rankings for the major IC foundries. According to IC Insights, Texas Instruments was the fifth-largest foundry in 2007. IC Insights top-ten foundry ranking for 2007 includes the pure-play foundries TSMC (Taiwan), UMC (Taiwan), SMIC (China), Chartered (Singapore), Dongbu (South Korea), Vanguard (Taiwan), and X-Fab (Germany); and IDMs Texas Instruments, IBM and Samsung.

54 The location of X-Fab headquarters is in Erfurt, Germany. It has about 2,600 employees, and manufacturing sites in the US, the UK, Malaysia, and Germany.

Table 3: Top 10 foundries by revenue, 2007

Top 10 Foundries by Revenue, Worldwide, 2007 (Millions of Dollars)

Rank 2006	Rank 2007	Company	Revenue 2006	Revenue 2007	Growth (%) 2006-2007	Market Share (%) 2007
1	1	TSMC	9,716	9,828	1.2	44.3
2	2	UMC	3,191	3,263	2.3	14.7
4	3	SMIC	1,465	1,550	5.8	7.0
3	4	Chartered Semiconductor	1,527	1,445	-5.4	6.5
5	5	IBM Microelectronics	688	605	-12.1	2.7
8	6	Vanguard	398	488	22.6	2.2
10	7	X-Fab	293	411	40.3	1.9
6	8	Dongbu HiTek	462	405	-12.4	1.8
7	9	MagnaChip	404	370	-8.4	1.7
9	10	Hua Hong NEC	300	321	7.0	1.4
		Top 10 Total for 2007	**18,444**	**18,686**	**1.3**	**84.2**
		Others	3,201	3,506	9.5	15.8
		Total Market	**21,645**	**22,191**	**2.5**	**100.0**

Source: Gartner (April 2008).

The foundry industry is heavily concentrated, the leading firm, TSMC, having a market share of over 40 percent. TSMC currently employs over 20,000 people worldwide. Historically, Taiwanese firms have dominated the independent foundry industry since its formation. It is, however, notable that China is rapidly catching up: SMIC, now the third largest foundry firm, built its first foundry in 2001. China has now three foundries among the top 14. Semiconductor firms have specifically been promoted by policies in China, including the internationally debated Circular Number 18, which reduced the VAT rates of Chinese semiconductor firms to maximum 6 percent, and then lowered the tax burden to 3 percent.[55] We discuss developments in China in more detail in the next chapter.

Before the global downturn was clearly visible, the Fabless Semiconductor Association (now Global Semiconductor Alliance) predicted that, from 2006 to 2011, pure-play foundry sales display a 15 percent compound annual growth rate (CAGR), almost double the eight percent total IC industry expected CAGR during the same time frame. In contrast, the IDM foundry business was forecast to grow at a rate of 12 percent. Pure-play foundries were forecast to represent 85 percent of total foundry sales in 2007.[56]

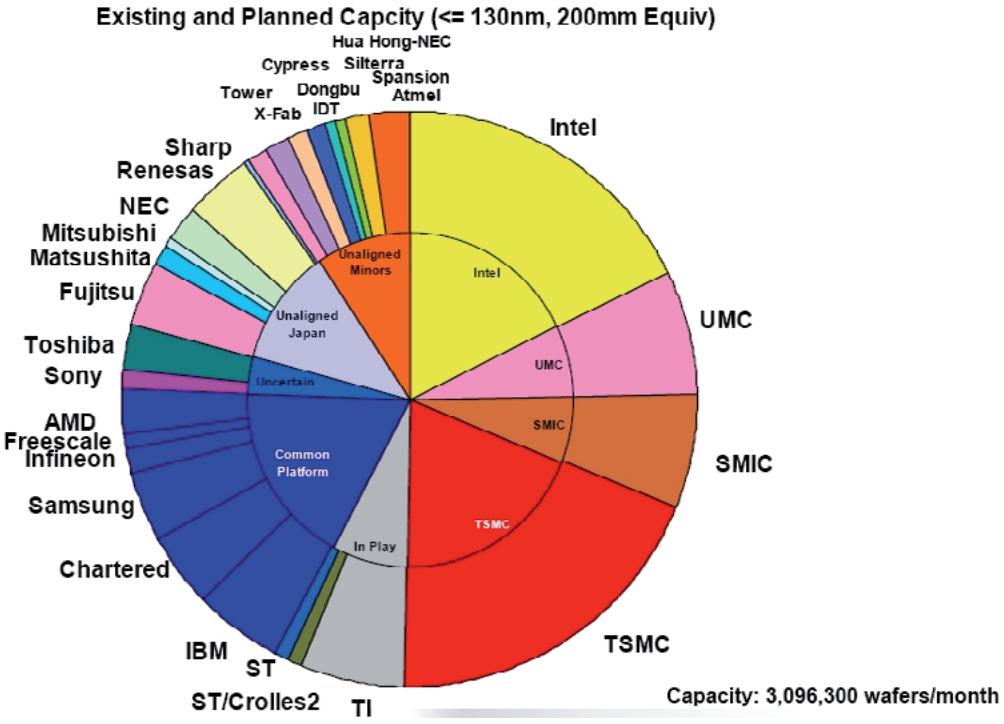
The overall worldwide foundry capacity and the main alliances in 2007 are shown in Figure 3.[57] As the picture shows the actual foundry capacity, including capacity that is used internally, firms such as Intel and Samsung take big slices of the total pie. Samsung, in fact, also has an independent "pure-play" foundry that provides capacity to outside customers. Since 2007, the alliances have continued to be shaped and, for example, Toshiba, STMicroelectronics,

55 Cf. "China's Semiconductor sector shake-up", People's Daily Online, September 8, 2004. Circular 18 created loud protests both in the US and EU, and tax rules for semiconductor industry have since been modified. The new Chinese Corporate Tax Income law is discussed in detail below.

56 FSA Semiconductor Market Report, October 2007.

57 Kunkel (2007).

Figure 3: Alliance landscape in semiconductor wafer manufacturing



Source: Kunkel (2007).

and the new AMD-ATIC foundry company have joined the Common Platform alliance.

4.1.2.4. Fabless firms

Many IDMs have drifted towards the fab-lite and fabless model during the last years. This has been possible because of the increased capacity and capabilities of pure-play foundries. The growth of pure-play foundries, in turn, mainly results from the rise of new fabless semiconductor firms that focused on chip design. In 1989, almost 70 percent of all memory, logic and processor chips were produced for the PC market. Since the early 1990's, mobile communications, computer games, audio, and image processing have become important end uses for ICs. Often these applications require design capabilities for both digital and analog electronics, as well as processing of real time data streams.

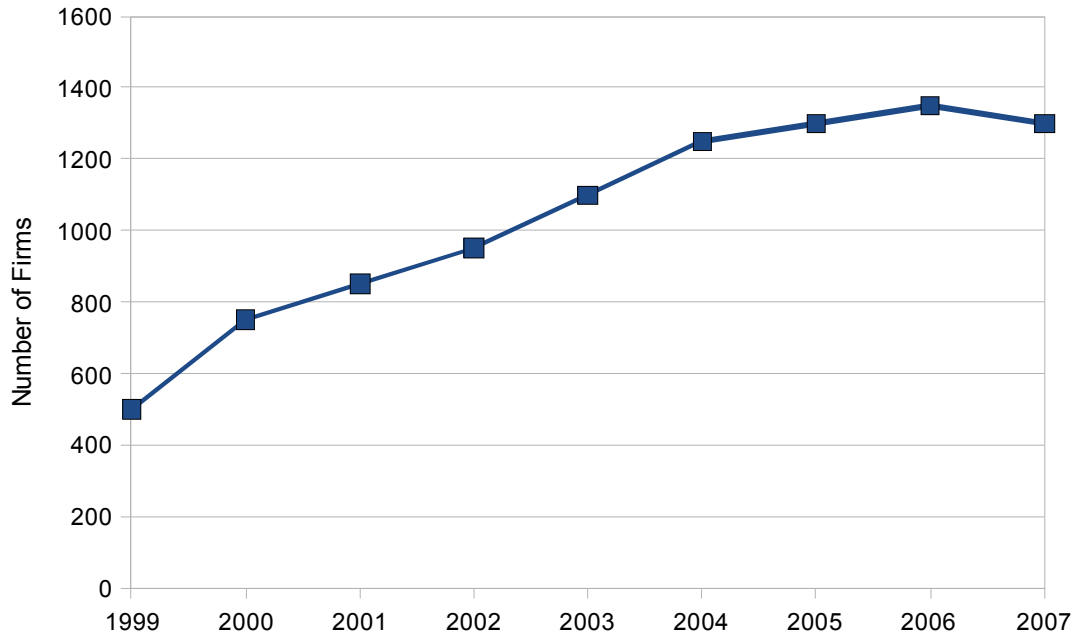
Due to the small initial size of these markets, lack of interest from large IDMs, and relatively high costs of customized manufacturing, a large number of specialized IC design houses emerged in the 1990s. When they started to sell their ICs to electronics equipment manufacturers, they had to search for outsourced wafer fabrication capacity. At first, this was provided by the IDMs, at times when their own capacity utilization rates were low. In general, this was a difficult business niche, as small IC firms were low on the priorities of the IDMs.[58]

The emergence of independent pure-play foundries, including TSMC and UMC, changed the picture radically. Fabless firms that never have had their own wafer manufacturing capability now include important semiconductor firms, such as Qualcomm, Xilinx, NVIDIA, Broadcomm, and Creative.

There are now several hundreds of fabless firms worldwide. Future Horizons classifies 121

58 Shelton (2001); and Dhayagude,T., M. Jayagopal, T.J. Manayathara, S. Suri, and A. Yaga (2001).

Figure 4: Fabless semiconductor firms, 1999-2007



Source: GSA, 2008.

Table 4: Top 20 semiconductor vendors in 2008

Rank	Company	Headquarters	Business model
1	Intel	US	IDM
2	Samsung	South Korea	IDM / Foundry
3	Texas Instruments	US	IDM / Fab-light
4	Toshiba	Japan	IDM
5	TSMC	Taiwan	Foundry
6	STMicroelectronics	Europe	IDM
7	Renesas	Japan	IDM
8	Hynix	South Korea	IDM
9	Qualcomm	US	Fabless
10	Sony	Japan	IDM
11	Infineon	Europe	IDM
12	AMD	US	IDM / Fabless
13	NEC	Japan	IDM
14	Micron	US	IDM
15	NXP	Europe	IDM
16	Freescale	US	IDM
17	Fujitsu	Japan	IDM
18	Broadcom	US	Fabless
19	Panasonic	Japan	IDM
20	Nvidia	US	Fabless

Source: data from IG Insights, 2008.

semiconductor firms in Europe and Israel as fabless companies.[59] According to the Global Semiconductor Alliance (GSA), there were 600 fabless firms in North America, 150 in Europe, 500 in Asia, and 50 in Israel in year 2007. According to GSA, the public fabless revenue totalled USD 53.1 billion, or about 20 percent of the global semiconductor sales in the same year. The total number of fabless firms, as reported by GSA, is shown in Figure 6.

The largest semiconductor producers are listed in Table 4, which also shows the core business models and headquarter locations of the firms. The ranking is based on sales in the first three quarters in 2008, as reported by IC Insights.

As can be seen from the table above, IDMs are still the largest semiconductor vendors, when ranked using their sales revenues. This is, however, somewhat misleading as the different business models cannot really be compared simply by using the generated revenues. Part of the attractiveness of the fabless model is the fact that foundries can amortize their plant and R&D costs among many customers. To be viable, IDMs need to generate more revenues than fabless firms to cover their higher costs in fixed assets. The IC Insight rankings also include pure-play foundries, such as TSMC, which represent inputs to the device producing industry. The largest fabless firm in the table, Qualcomm, also gains much of its revenues by licensing its technology to IDMs. In fact, Qualcomm combines two different business models; it is both a traditional fabless integrated device manufacturer and a "chipless" semiconductor firm that sells patent rights and designs, instead of finished products. The next section provides an overall view of the chipless model. The following sections then discuss this model and its variations in more detail.

4.1.2.5. Chipless IP firms

The key characteristic of the semiconductor IP business is that it does not transfer ownership; instead, semiconductor IP firms sell rights to use and copy the designs. The designs are called with various names, including "virtual components," "IP blocks," and "IP cores." The revenue streams typically originate in license fees that can be one-time, annual, based on the number of customer designs that use the licensed IP, or a mixture of these; royalty payments that are calculated based on the number of products that the customer has shipped which include the licensed design; and complementary services, such as training, technical support, customization, and development tools. As the product is an intangible product, the terms of sale can be defined as a business contract. For example, the vendor may restrict the use to specific geographic markets, industry segments, or, for example, for products that do not compete with the vendor's other products.

Typical semiconductor IP licensing models are shown in Table 5.

Semiconductor IP blocks are licensed by many different types of firms. Foundries provide large libraries of pre-designed and pre-tested IP that is optimized for the foundry's fabrication process. Such foundry IP often consists of basic logic components and "standard cells," and also more complex IP cores developed by third-party IP vendors, and it is often available for customers without license or royalty fees. Similarly, design tool vendors typically provide large libraries of pre-designed IP with their design software. In recent years, also IDMs and fabless semiconductor firms have increasingly started to license their in-house developed reusable designs.

A special case among fabless firms is the FPGA vendors, including the market leaders Xilinx and Altera. FPGA chips provide a platform onto which different designs can be downloaded. As the complexity of implemented designs has

59 Future Horizons: The European Fabless Semiconductor Report, 2007 Edition.

Table 5: Typical semiconductor IP licensing models.

	Per Use	Time Based	Royalty Based	Access Based
Purpose	Fee for each IP on defined user scope	Multiple uses over a period of time	Share risk and reward	Fee for an IP portfolio over a period of time
Payments	Event Based	Time Based	Value Based	Subscription Based
Structure	One time fee	Fee for all designs within a given time	Some or all fees spread across units	Up Front Fee plus discounted use fee
Scope	Per Design Per Device	Multiple Uses Per Device	% of Device Value	Multiple IPs per Organization

increased, designers now typically use IP blocks provided by the FPGA vendor as components in their designs. These IP blocks are typically optimized for the FPGA chip in question, and range from vendor-developed embedded processor cores to cost-free entry-level cores that are bundled with the FPGA vendors design tools and development boards. FPGA suppliers also have extensive partnership projects for independent IP vendors who target their designs for the suppliers FPGA technology.

The semiconductor IP industry therefore consists of a large variety of rapidly evolving business models. At one extreme is the "pure-play IP" or "chipless" model. Pure-play IP vendors do not have their own semiconductor device products; instead they focus on creating and licensing designs to chip designers. Typically, IP blocks are used by independent design service firms and fabless semiconductor firms, and they are also licensed by traditional IDMs.

Due to the rapid evolution and large variety of the IP business models, market analysts and experts use many alternative definitions and sometimes incompatible terminology in describing the IP industry. IP blocks can contain digital or analog circuitry, or a combination of these. Digital components are used to design logic functions and complete systems-on-chip. Analog components, in turn, are used, for example, to convert real-world signals such as radio waves and sensor data into digital format. Three main categories of digital IP components are commonly distinguished. These three types of components roughly map with the outputs of the three main steps in the digital chip design process: functional specification, logic design, and physical design.

Soft cores are IP blocks that describe the functionality of the IP component. Soft cores are usually delivered using high-level hardware description languages derived from computer programming languages.[60] A soft core, therefore, typically consists of a set of text files that contain the "source code" for an IP block. When a high-level specification is provided, the specification can further be "compiled" into a lower-level "netlist" that describes how the underlying elementary logic components or "gates" are connected. This generation of logic "circuitry" from a higher level hardware description is known as logic synthesis. Soft cores that are delivered in a hardware description language format are therefore also known as synthesizable cores. The lower-level netlist format is also widely used to deliver soft cores. The netlist format is mainly used because it protects the vendor's trade secrets and intellectual property better than the higher-level source code.

Soft cores are typically independent of the specific manufacturing process used to make the chips. Soft cores define the architecture and functionality in a form that can be read by synthesis tools that convert the description into

60 The two main hardware definition languages are VHDL, derived from the ADA programming language, and Verilog, derived from the C programming language.

features on semiconductor die; typically, however, the design incorporates very little information on the physical layout or the specific requirements of a manufacturing technology to be used to make the chip. Soft cores are also widely used to configure FPGAs. It is, for example, possible to download a complete microprocessor architecture onto a FPGA chip. Such soft microprocessors are provided by the FPGA suppliers and they are also available as open source code. A common scenario is that a new custom-designed semiconductor is first implemented using a FPGA chip and later manufactured in higher volumes as an ASIC chip. As IP cores that are optimized for FPGAs can rarely be used as such on ASIC designs, both FPGA vendors and foundries provide services that help in translating the designs from one platform to another.

The major advantages of soft cores include their customizability. A soft core is specified in high-level description language that looks like source code for a computer program. Its functionality, therefore, is relatively easy to modify and can be configured according to the specific needs of the user. As the core is delivered in a form that is typically independent of the specifics of the manufacturing process, the same core can with some translation effort be manufactured in many different processes. This means, for example, that the user can source the manufacturing from competing semiconductor foundries.

Hard IP cores, in contrast, are closely tailored to the specific manufacturing process used to make the chip. Hard IP cores, also known as hard macros, are delivered in the form of a mask-level layout.[61]

Hard IP cores have the advantage that they require little extra work before they can be implemented on a semiconductor die. The logic gates are arranged in a specific geometric pattern that takes into account the characteristics of the wafer manufacturing process to be used in production. The exact size the core will need on the die, its power consumption, and other physical characteristics including speed and operating temperature are also known. Hard IP cores are often also used for analog and mixed-signal logic cores, where physical characteristics are important for the design. Hard cores, therefore, are widely used, for example, in multimedia devices and mobile phones.

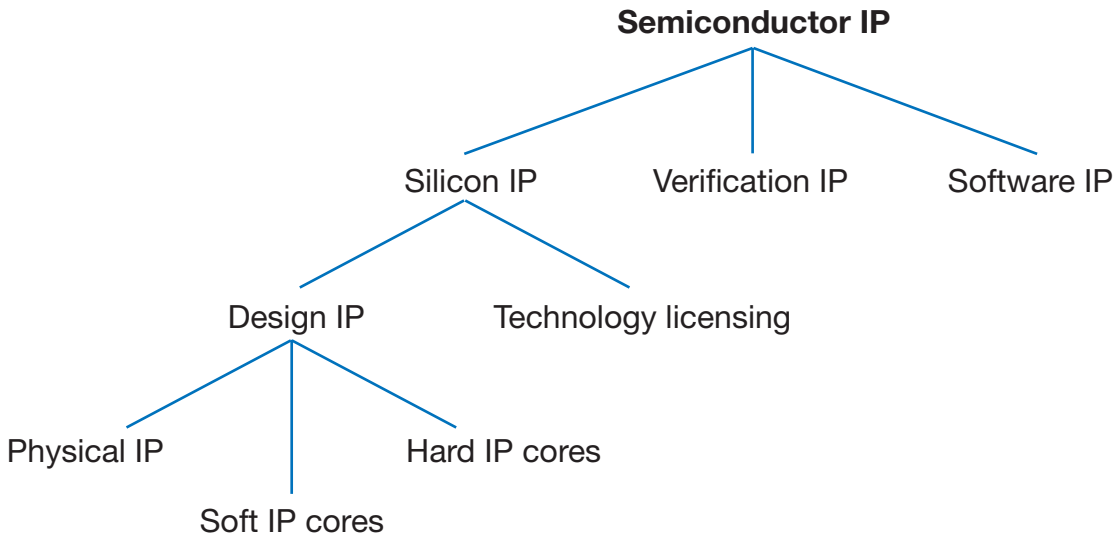
The main benefit of hard IP cores is that they can be pre-tested in a specific manufacturing process. This typically means faster time-to-market with less risk and less development cost. As a hard IP core is optimized for a specific manufacturing process, it is, however, usually impossible for the end-users to modify or configure hard IP cores. When leading-edge chips are manufactured, the physical characteristics of the design become very important. In practice, cores for leading-edge manufacturing process technologies are, therefore, hard cores.

The third main category of pre-designed IP components consists of *physical IP components*. Physical IP components typically have relatively low functional complexity, and they provide the basic building blocks such as standard logic functions, also known as "standard cells," and basic input-output IP and memory compilers that generate on-chip memory blocks. Physical IP components are always optimized for and tested in a specific manufacturing process. Designers can use libraries of physical IP to build more complex functions, IP cores and even complete systems-on-chip.

IP cores and physical components form the basic products of the semiconductor IP design industry. To cover the broader IP ecosystem, the industry is also sometimes divided into three complementary segments, one comprising

61 More accurately, they are delivered as data files that describe the layout. The data files typically use the industry-standard GDS II stream format, or the newer OASIS format supported by SEMI.

Figure 5: Types of semiconductor IP



Source: Meaning Processing

of "silicon IP" that focuses on the actual semiconductor designs; another comprising of "verification IP," including libraries of test cases that are used to check that created designs perform according to standards and specifications; and a third segment that consists of software, such as hardware-specific drivers, algorithms, operating systems, and development tools. Silicon IP, in turn, is sometimes sub-divided into two segments: "design IP" that consist of IP cores and physical components, and "technology licensing" that focuses on patent licensing.

A schematic representation of these semiconductor IP classes is shown in Figure 5. Leading firms typically provide a combination of products in these different categories. For example, ARM has separate divisions for IP cores, physical IP and software. Rambus, in turn, generates revenues from licensing its patented technologies, while also supplying design IP based on the same technologies.

A large number of chipless firms exist today. The Design And Reuse web site lists about 400 silicon IP vendors.[62] Chipestimate, in turn, lists 193 IP vendors as its partners.[63] The Future Horizons 2007 European Fabless Report lists 72 European chipless firms.[64] Many of these firms are very small. Industry insiders estimate that top 10 vendors represent about 70 percent of total semiconductor IP revenues, and that the next 150 firms have revenues around USD 1.5 million, on average.

Europe has some important first-tier chipless firms, including ARM (£298.9 million in revenues in 2008), Imagination Technologies (£64.1 million in 2009), and ARC International Ltd. (£17.0 million in 2008). The chipless market and vendors are described in more detail in the following chapter.

The boundaries between design houses, chipless firms, fabless firms, and design software vendors are blurred ones, and also many IDMs, foundries and electronics firms sell IP blocks to the semiconductor community. The accuracy of data about this segment is often limited both by definitional challenges and data availability. For example, the In-Stat/MDR study[65] on the

62 http://www.design-reuse.com/

63 http://www.chipestimate.com/
64 ibid.
65 In-Stat/MDR (2004) Independent IP Logic Market, August 2004.

independent IP logic market excludes the design software and IP vendor Synopsys, whereas Gartner market share analysis list Synopsys as the third largest design IP vendor worldwide. Including IP block revenues of large design software vendors and non-logic IP vendors, Gartner adds the total world market for semiconductor design IP in 2007 to USD 1,4 billion, and technology licensing up to USD 550 million. The preliminary numbers for 2008 are USD 1,486 for design IP and 587 for technology licensing. The detailed breakdown was shown in Table 1.

Not all semiconductor IP is visible in market studies, however. As was noted before, perhaps over 80 percent of reusable IP is created inside semiconductor and electronics firms, and never sold to outsiders. Also open hardware projects, inspired by successful open source and open content initiatives, have created numerous IP cores that are licensed for free, typically using GPL or BSD -type licenses. Initiatives in this area include OpenCores.org,[66] Open Collector,[67] the Hamburg VHDL archive,[68] and the OpenSparc.net.[69]

As was pointed out before, the revenues of chipless firms cannot really be compared with IDMs or fabless semiconductor vendors. Traditional semiconductor device producers, including fabless firms, use the outputs of chipless IP firms as their inputs. The IP creation activity, however, is the key source of value in the semiconductor industry. Developments in the chipless segment can therefore potentially reorganize the value system in the semiconductor industry. More importantly, the emergence of reusable designs as a separate product category can also have profound consequences for innovation models that underlie developments in the broader ICT industry and, thus, for the entire knowledge economy.

4.1.3. The Semiconductor Value Chain

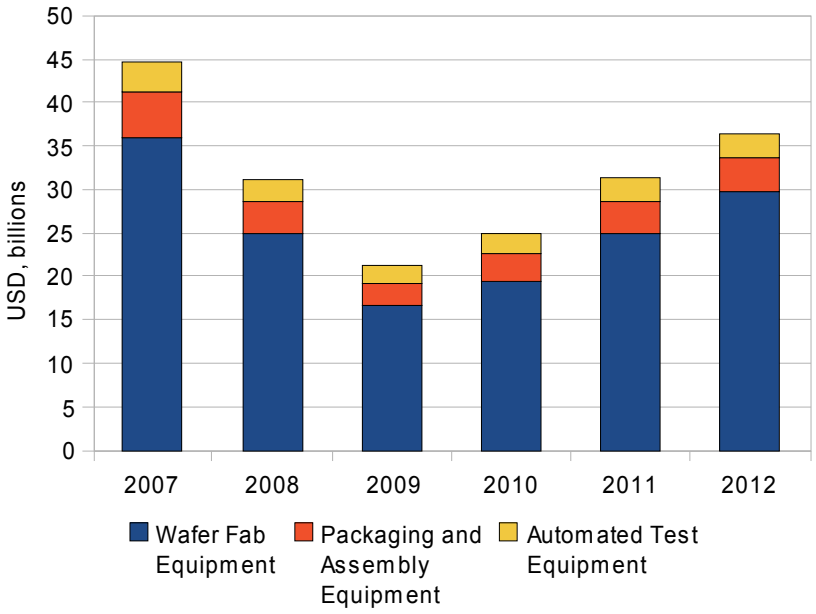
The semiconductor value system consists of firms that follow the above discussed business models, as well as several other key actors. These include electronic design automation (EDA) tool suppliers, semiconductor assembly and testing services (SATS), semiconductor manufacturing equipment suppliers, lithography photomask merchants, silicon wafer suppliers, and other materials suppliers. In this section we briefly map the main segments of the value chain.

Integrated circuits are created in a very disaggregated and globally distributed network of activities. The basic starting point, however, is clear. To create a chip that can be used in an electronics product, the chip has first to be designed. Most of the design work is done internally by IDMs and fabless firms but design work is also increasingly outsourced and predesigned IP components are commonly used as noted above. The design service and IP market was about USD 2.8 billion in 2007.

The outputs of the design phase are used to create optical masks that are used to "print" microscopic components on silicon wafers. As modern chips can consist of tens of layers that need to be exactly aligned to produce a working chip, a set of optical masks required to expose a silicon wafer can easily cost over a million USD. The optical mask manufacturing processes are highly automated, and the equipment are supplied by a relatively small number of firms that apply sophisticated technologies and state-of-the-art knowledge to make the manufacturing process possible. Mask making is also nowadays a very computer intensive task. In the advanced semiconductor fabrication processes, where the wavelength used to expose the mask image onto the wafer greatly exceed the desired feature sizes, masks are computed so that their interactions with the actual fabrication process create the desired features on the wafer. In the bleeding-edge, the mask features are purely computational, with no

66 http://www.opencores.org/
67 http://www.opencollector.org/
68 http://tams-www.informatik.uni-hamburg.de/vhdl/
69 http://www.opensparc.net/

Figure 6: Semiconductor equipment spending, 2007-2012



Data from Gartner, Inc., 2008

visual correspondence with the image produced. Today, many semiconductor manufacturers outsource mask making to specialist firms. This merchant photomask market was about 2.3 billion USD in 2007.

Similarly, polished semiconductor wafers are produced by firms that specialize in growing silicon crystals. Although wafers represent the most critical raw material for the industry, in the sense that the wafers provide the actual physical substance onto which chips are formed, the industry also uses many other materials, including an increasing number of rare metals, and gases such as helium and silane. For example, the market for photoresists was about USD 1.2 billion in 2007. In total, the semiconductor materials market was about 28 billion USD in 2007, and roughly half of that, about 12.5 billion, was for silicon wafers.

At present, about 25 percent of the cost of setting up a semiconductor factory consists of optical lithography machinery that is used to expose the wafers. The future generation extreme ultraviolet (EUV) lithography machines are expected to cost about USD 100 million per unit, or more than a Boeing 737.[70] In total, the semiconductor manufacturing equipment industry had revenues of about 45 billion USD in 2007. The capital equipment spending declined dramatically at the end of 2008, and Gartner, Inc. now expects equipment spending to contract to 21 billion in 2009. The capital equipment spending breakdown is shown in Figure 6, based on December 2008 data from Gartner, Inc.[71]

After semiconductor wafers are exposed and processed, they are cut into chips that are further wired and packaged into components. As the creation of semiconductor wafers is difficult, typically only a fraction of the dies in a wafer are flawless. The dies, therefore, are tested in several ways before they are processed further. Today, packaging, assembly and testing are

70 The comparison comes from Risto Puhakka from VLSI Research.

71 Semiconductor Equipment and Materials International (SEMI) gives a wafer processing equipment market of USD 31.95 billion, assembly and packaging USD 2.84 billion, test equipment 5.06 billion and other equipment 2.92 billion, with total 42.77 billion for 2007.

widely outsourced to specialized SATS firms, mainly located in Asia. According to Gartner, semiconductor assembly and testing services was about a USD 20.6 billion industry in 2007. The top vendors include ASE Group, with revenues of USD 3 billion and market share of 15 percent, Amkor Technology (USD 2,7 billion), SPIL (USD 2 billion), STATS ChipPAC (USD 1.6 billion), and UTAC (USD 756 million). The SATS industry has been one of the growth segments in the semiconductor value chain during the last seven years.

The design of semiconductors relies today on sophisticated software tools that can be used to support the functional design of chips and their layouts. Due to the complex nature of even relatively simple semiconductor chips, it is impossible to create them without specialized computer-aided engineering (CAE) or electronic design automation (EDA) tools. The market is dominated by four US companies, Synopsys, Cadence, Mentor Graphics, and Magma Design Automation, although a large number of smaller specialist EDA vendors also exist. According to data from EDA Consortium Market Statistics Service, global revenues for CAE products were about USD 2.3 billion in 2007. In addition, the EDA industry gets revenues from IC physical design and verification tools, printed circuit design tools, design services, and semiconductor IP licensing. According to EDAC, the total revenues were about USD 5.8 billion, of which about 1.0 billion was for semiconductor IP.[72]

The users of CAE tools are the actual designers of semiconductor components. These design activities occur in various points of the semiconductor value system. For example, IDMs employ large numbers of design engineers. Large electronics manufacturers such as Sony, Samsung, Nokia, Motorola, and Philips have traditionally had large captive design groups developing application specific integrated circuits for their own products, although recently they have started to spin off and outsource much of their design activities. Independent design service houses such as the Indian Wipro and the Taiwanese Global Unichip Corporation now provide services for semiconductor design, and there are hundreds of small specialized design houses around the world. Also electronics manufacturing services (EMS) firms, such as Flextronics, have extended their services by providing semiconductor design services as part of their service package.

72 EDAC collects data from its member firms and complements it with data from other sources. The exact data collection methodology is not known but the IP data probably include some revenues from independent IP vendors.

Design Services for Future Technologies

Global Unichip Corp. (GUC), is a dedicated full service SoC (System On Chip) Design Foundry based in Taiwan. It was founded in 1998. GUC provides total solutions from silicon-proven IPs to complex time-to-market SoC turnkey services. GUC provides the most advanced silicon solutions through close partnership with the leading pure-play foundry TSMC, GUC's major shareholder, and other key packaging and testing power houses. With state of the art EDA tools, advanced methodologies, and experienced technical team, GUC promises to ensure the highest quality and lowest risks to achieve first silicon success. GUC has established a global customer base throughout Greater China, Japan, Korea, North America, and Europe. Revenues for GUC were about 295 million USD in 2008, representing an annual growth of 33 percent.

GUC works closely with TSMC, and they are therefore able to develop design tools and verify their semiconductor IP for bleeding-edge technologies ahead of competition. GUC is currently working on developing a 32nm test chip, which they expect to be out in 2009.

GUC has recently established branch offices in Europe and Korea, stating the need to be close to important competitors and big ASIC users.

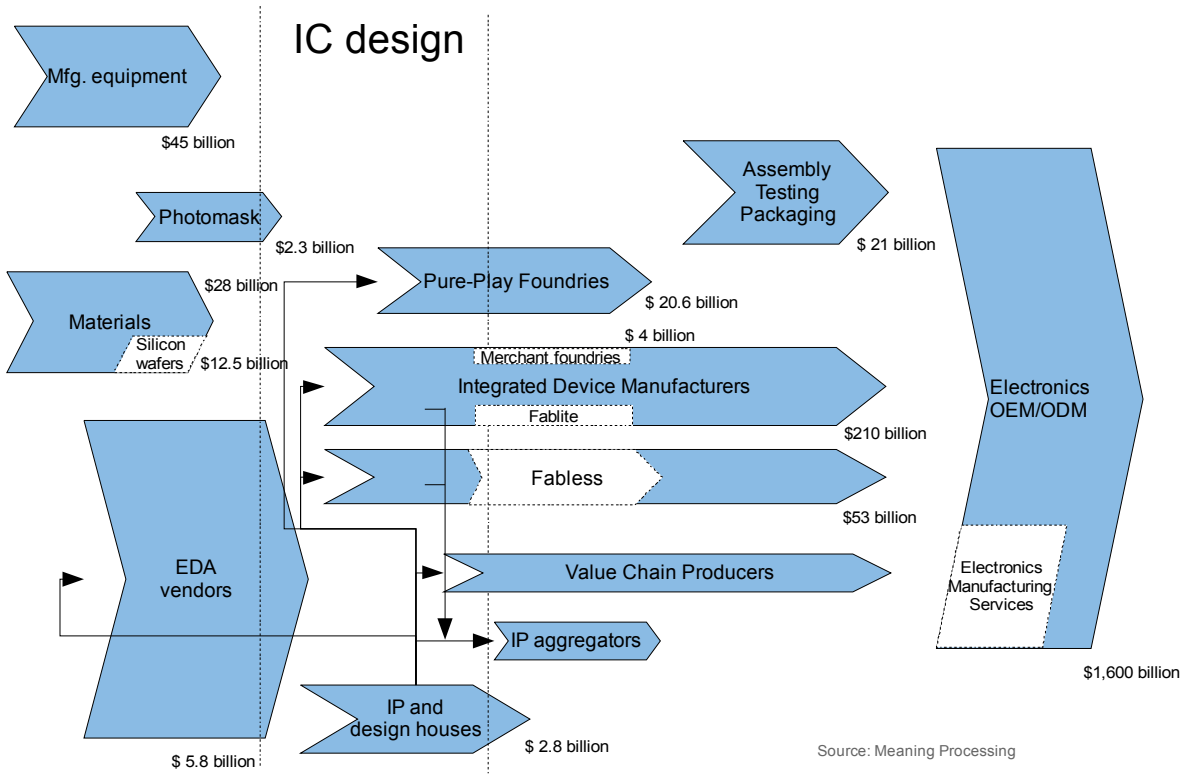
The semiconductor value chain with 2007 revenues is shown in Figure 7. In practice, firms can reconfigure their value adding activities in many different ways. For example, some IDMs and fabless firms develop their own CAE tools and they also license internally developed semiconductor IP components to outside customers. A relatively new phenomenon is also the emergence of manufacturing service firms that manage the creation of customer chips from design to integration of third-party IP, coordinating work with foundries and assembly and test firms. An example of such "value chain producer" is eSilicon, based in Sunnyvale, California.

IP aggregators are service firms that provide access to third-party semiconductor IP. Two important aggregators are Design & Reuse, based in Grenoble, France and ChipEstimate.com, based in San Jose, California.[73] Both allow the users to search for third-party IP components, and they also act as news portals. Design & Reuse also allows potential IP buyers to request new IP components from the pool of suppliers. A different type of IP aggregator is IPextreme. It focuses on licensing semiconductor IP that has been developed in IDMs and OEMs.

The independent semiconductor IP vendors are discussed in detail in the following chapter.

73 ChipEstimate was acquired by the EDA vendor Cadence in March 2008.

Figure 7: The semiconductor value chain, 2007.



Source: Meaning Processing

Electronics Manufacturing Services for Chip Makers

eSilicon is an electronics manufacturing service for semiconductor manufacturing. It calls itself a Value Chain Producer (VCP). It provides a comprehensive suite of design, productisation and manufacturing services, managing the production of devices for companies who don't want or are unable to deal with the complexities of the semiconductor value chain. The company delivers chips to system OEMs and fabless semiconductor companies.

Prior to 2000, electronics companies that didn't own their own semiconductor fabrication facility had two choices for the development and manufacture of their application-specific integrated circuits (ASICs). They could work with a large integrated device manufacturer (IDM), which locked them into limited facilities and a narrow intellectual property (IP) portfolio; or they could attempt to manage the process themselves by working directly with a pure-play foundry, and take on the associated risks and challenges.

eSilicon provides a third alternative. In this model, eSilicon offers a wide variety of design services; a broad portfolio of proven IP solutions and tools; and a full range of manufacturing support, including the delivery of packaged, tested chips. eSilicon creates an optimized semiconductor Value Chain for each customer and each design - from design services and tools, to IP and materials vendors, to test and packaging providers. It can take customer-created layout data files and manage the fabrication, packaging, test and delivery of the final silicon; a netlist and perform the physical design, and manage all subsequent manufacturing operations, including fabrication, packaging, test and delivery; or a completed IC design and provide full production support, including planning, supplier management and qualification, delivery flexibility programs and supply chain visibility.

eSilicon was founded in 2000, and it has about 115 employees. It was named 'Rising Star' in Deloitte's Technology Fast 500 program, January 2006.

In December 2007, eSilicon acquired the existing products and certain assets of the Swedish fabless firm SwitchCore AB. Through this acquisition, eSilicon extended its production services business model to the customers of companies that have made a decision to exit all or part of their existing businesses. Through this new service, eSilicon is able to extend the availability of these product lines by providing a continued supply of devices for the systems which incorporate them. This saves the customers of these product lines the financial and supply risks associated with the end-of-life buys they would have otherwise faced had the products been obsolete.

5. The Intellectual Property Business

5.1. The IP Market

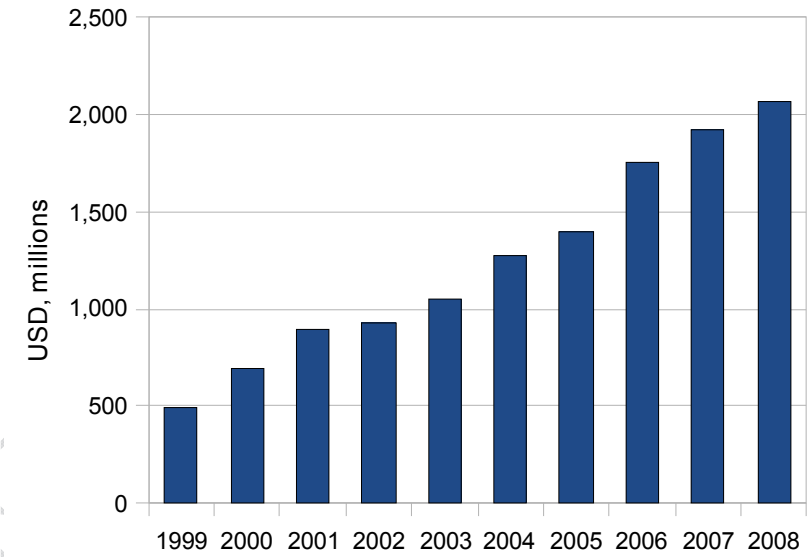
Different definitions of revenue streams and different methodologies lead to somewhat different estimates of the semiconductor intellectual property market size, at present giving estimates ranging from the low one billion USD[74] to over two billion USD. As there are many small vendors and many firms are privately owned, market studies are based on estimates. More importantly, different studies differ as they include different firms and revenue categories. For larger firms, revenues also greatly depend on how they book revenues from license and royalty contracts and exceptional income from legal settlements.

74 EDAC Market Statistics Service gives 1,043 million USD revenues for 2007, excluding IC physical design and verification (valued at $1,567 million) and services ($337 million). EDAC MSS collects mainly data through the partner organizations of the EDA Consortium; in the IP area it, however, uses also "available public sources," without detailing them.

The global revenues from semiconductor IP, including technology licensing and design IP, are shown in Figure 8 using data from Gartner, Inc.

Market researchers do not always describe their data collection methodology in detail, and it is therefore difficult to know how exact the numbers are. In particular, it is not obvious how the market for foundry IP and IP provided by EDA firms should be counted. Major IP vendors also get revenues from design services, consulting, training, and design software. An independent verification of the revenues of the top 20 IP vendors, using public filings in 2007, complemented with the estimated volume for the about 450 firms that actively market their IP, leads to an estimate of USD 1.8 billion in 2007, which is close to Gartner estimate of 1.9 billion. The revenue structures are discussed in more detail below. According to preliminary data from Gartner, Inc., the IP market will be 2.1 billion in 2008, growing 7.7 percent from 2007.

Figure 8: Semiconductor intellectual property market, 1999-2008



Source: Gartner, Inc., various years.

The microprocessor IP market will be USD 582 million, and digital signal processing IP market about 52 million.[75]

The estimated growth of the semiconductor IP markets is shown in Figure 9. The data for the figure comes from iSupply, 2007. As recently as in June 2008, Gartner, Inc. expected the independent IP and chip design services to grow at a compound rate of 11.4 percent from 2007 to 2012, to reach USD 4.8 billion at the end of the period. The rapid economic downturn towards the end of 2008 will lead to revised estimates, perhaps cutting the 2009 revenues down in the 25 percent range. This will most probably lead to the exit of many small IP vendors, many of which have difficulties in finding financing for their unprofitable operations.

75 See Table 1.

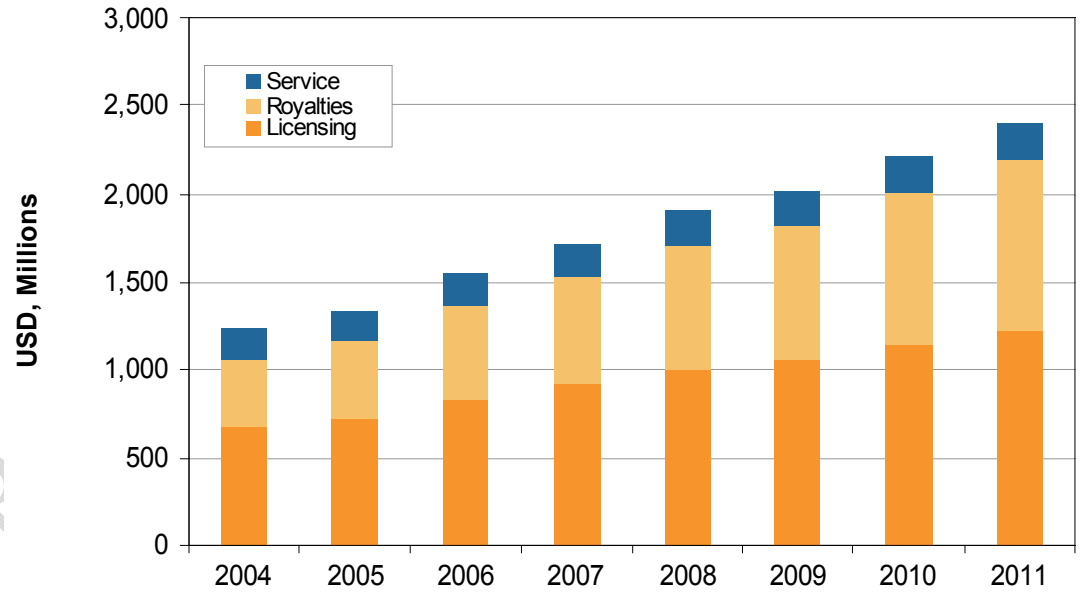
5.2. IP Customers

Semiconductor IP is purchased by three main customer groups. The most important of these is integrated device suppliers. Both fabless semiconductor firms and IDMs use third-party IP to create new devices. For example, Intel has licensed ARM's processor cores since 1997, and both Qualcomm and Texas Instruments use ARM cores in their mobile phone chips.

Second, semiconductor IP is also licensed by electronics manufacturers who develop their own ASICs and SoCs, or who need access to patented technologies.

Third, semiconductor IP is licensed to design houses, who design systems and chips for equipment manufacturers, and to independent IP vendors, who develop their own software, semiconductor, and verification IP that can be combined with the purchased IP. Although small design houses and IP vendors create relatively small revenue streams, major IP vendors actively support this customer group. This is because the

Figure 9: iSuppli semiconductor IP revenue forecast, 2004-2011



Source: iSuppli, 2007

success of an IP core and its broader architecture typically depends on vibrant ecosystems of third-party developers and designers.

In many cases, the IP licensee could also use its internal design team to create the required IP, or outsource the design task to a design service firm. The make or buy decision is influenced by factors such as time-to-market, cost, availability of competent engineers, the competitive advantages created by proprietary designs, and product life-cycle considerations. Furthermore, as purchasing of IP cores requires both technical evaluation of the quality of the IP and the assessment of economic and legal risks, the purchasing process is often complicated. The main decision criteria, as perceived from a potential design IP purchaser's point of view, are outlined below in Table 6.

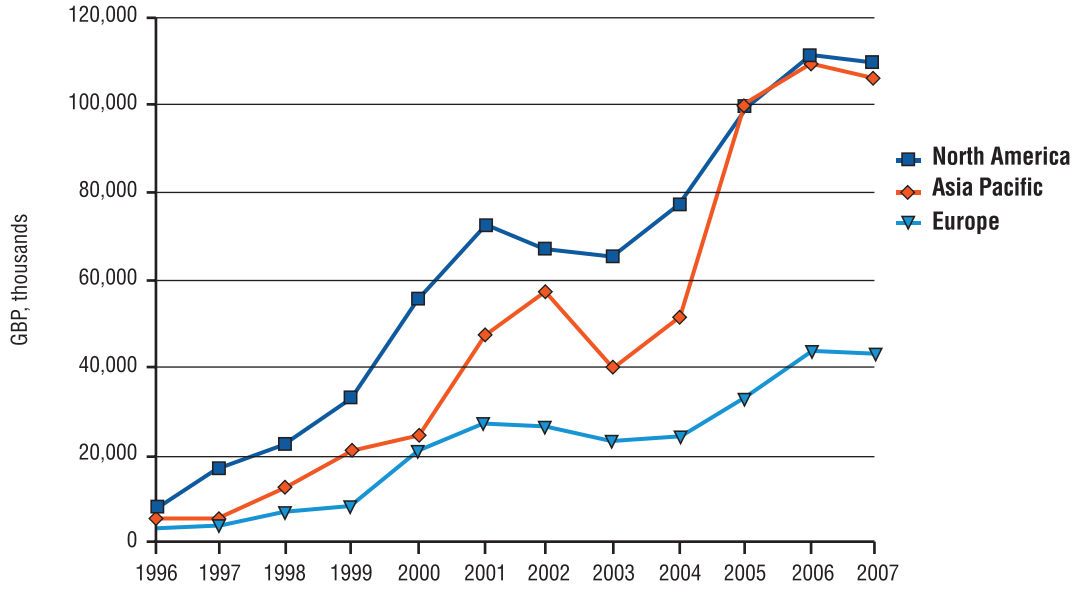
IP vendors typically have to address the above requirements if they want to be economically viable. In practice, they usually have to make trade-offs, and focus on customers whose demand matches with the characteristics of supply. In general, the economics in the semiconductor IP sector improve the competitiveness of the largest firms.

The globally leading IP vendor is ARM Holdings, plc. ARM has grown rapidly partly because it was able to provide processors that have been particularly suitable for mobile phones, and as

Table 6: Main criteria for semiconductor IP make-or-buy decisions.

Time to market	The main attraction of IP cores is that they can considerably accelerate product development and shorten the time to market. An IP core can embed several dozens of years of engineering effort. By reusing a core, much of this effort can be avoided, and a new product can be launched rapidly.
Availability of skilled designers	Semiconductor IP design requires sophisticated skills and experienced developers. When the IP addresses specialist domains, the designers also need expert knowledge in these application domains. Typically, the required skills are in short supply.
Development cost and commercial risk	Although commercial high-quality semiconductor IP is not necessarily cheap, it is almost always cheaper than if the same core would be developed internally. This is because IP vendors can usually amortize their development costs over many customers. Semiconductor IP contracts also typically consist of three cost components: one-time front-end license fee, support, and royalties. Royalty payments are bound to the number of final products actually shipped. If the product does not ship, there are no royalty payments.
Technical risks	IP cores are complex and the designs almost always have design errors and bugs. The majority of ASIC development costs is today related to the testing and verification of the designs. Commercial IP that is widely used has lower risks. The leading commercial IP cores are usually tested for several manufacturing processes in many foundries. They therefore have considerably smaller technical risks that designs that are implemented for the first time.
Legal risks	Internally developed IP can also have legal risks, as someone may claim that the designs infringe existing intellectual property rights.
Benefits from proprietary designs	Firms may want to develop IP internally if the design contains unique proprietary knowledge that can lead to competitive advantages. If the IP is widely available and does not differentiate products, there is little reason to develop it internally. Commercial IP may also be attractive if it contains unique functionality that could lead to competitive advantages, or if the vendor has patent rights to critical technological solutions.
Product lifecycle management	IP users typically plan for product lifecycles that consist of several product versions. If the IP vendor is able to invest in continuous improvements in its IP, the user may benefit from new innovation and technical advances.
Sourcing risks	When customers build their products using licensed IP cores, their products become dependent on these cores. The user may have problems if the core does not work as expected, or if the vendor is unable to maintain it throughout the end-product lifetime. Vendor reliability and financial and technical capabilities, therefore, are important factors when cores are licensed.
Vendor support	The integration of IP cores into new designs often requires experience and expert knowledge. IP users need to know whether the vendor can provide such expertise when needed.
IP ecosystems	Large IP vendors support third-party developers who build complementary IP, for example, compatible cores, verification IP and development tools. These can increase design flexibility and decrease economic and technical risks.

Figure 10: ARM revenues by customer location, 1996-2007

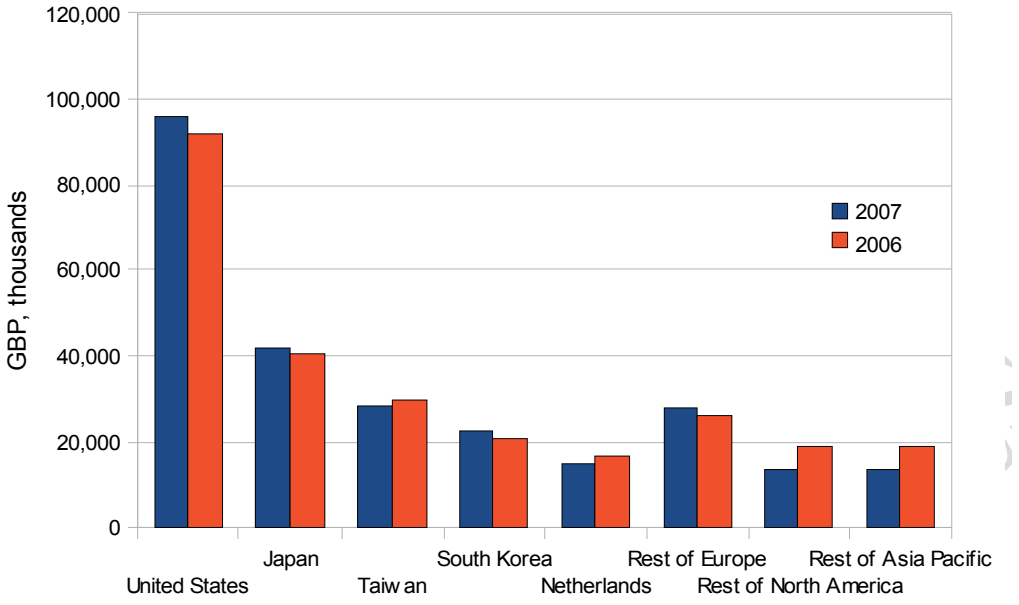


Source: Meaning Processing, 2008

the largest mobile phone maker Nokia decided to use third-party processors and chips in its phones. ARM revenues by destination, defined as location of customers are shown in Figure 10. The data come from ARM annual reports, 1998-2007.

A more detailed breakdown of ARM revenues by destination, defined as location of customers, for years 2007 and 2008 is shown in Figure 11.

Figure 11: ARM customer locations, 2006-2007



Source: Meaning Processing, 2008

5.3. IP Providers

In semiconductor design, intellectual property can be created as copyrights, mask works, and patents. Revenues can be generated by licensing the intellectual property, by collecting royalties when the IP is used, by providing complementary products and services, such as development tools and contract services, or by using IP internally to gain competitive advantages. IP vendors typically combine several of these revenue streams.

Most of the IP vendors are very small firms, often with less than five employees. The barriers for entry are low, as IP can be designed by anyone with access to a PC, design tools, and relevant design skills. Two types of small IP firms are common. In the first case, small independent IP vendors code some specialist knowledge about a specific application domain into a design that can be licensed. These IP firms often have their roots in universities where new ideas for electronic design or new algorithms have been developed. In the second case, small design houses start to sell their accumulated IP as an independent product. These firms typically have their roots in design expertise.

In the 1990s, there were great expectations that independent semiconductor IP firms would rapidly become the next big thing in the semiconductor industry. This did not happen, partly because of the ICT downturn in year 2000, but also because the independent IP vendor model is difficult to make economically viable for a number of reasons. First, as noted above, IP users need reliable and predictable vendors, who can provide support and maintain their IP as long as the user needs it. Such product lifecycle management typically requires considerable resources. Second, the users often need flexible and large portfolios of IP. Larger vendors therefore have a clear advantage. They have also an advantage if they can provide components that match well together and which can easily be integrated with each other. The smaller IP vendors often therefore try to join partnership programs set up by the key actors. An example of such IP ecosystem is the ARM Connected Community.[76]

Small successful design-oriented IP firms do exist. An example, Arteris, SA, is detailed in the box on the next page.

As firms in recent years have started to actively manage their intellectual capital portfolios, many firms have realized that they could benefit from licensing their semiconductor IP to outsiders. In practice, however, licensing typically requires considerable effort. For example, the IP has to be documented in a form that makes it useful for outsiders. In practice, the legal and managerial effort required to negotiate licenses also often exceeds the benefits of licensing IP designs. Semiconductor firms have therefore often used their IP in a form of patents. Large patent portfolios can be used both to limit competition and to improve their competitive position through cross-licensing. For example, Texas Instruments has used its IP to create chips for their customers and to limit competitor activity, but it rarely licenses its designs to external developers.[77] Also some independent IP firms have converted their business models toward patent licensing. An example, Patriot Scientific, Inc., is detailed in the second box on the next page.

Also large semiconductor firms gain considerable revenues by licensing patent rights. For example, a large fraction of Qualcomm's 9.7 billion USD revenues and over half of its 6 billion gross profit comes from patent licensing. Qualcomm, however, is not counted as an IP vendor in market studies. If it would license its IP cores, it would easily become the globally largest IP vendor.

76 http://www.arm.com/community/

77 In fact, the strengthening of the US patent rights, and the resulting increase in patenting, are often associated with the change in Texas Instruments patent policy in the early 1980s.

Arteris, Inc.

Arteris, Inc. is now headquartered in San José, California, with its main base in Paris. It was founded in February 2003 to develop and sell Network-on-Chip IP. Network-on-Chip (NoC) is used to link the various IP cores on a System-on-Chip in a somewhat similar way as the Internet connects computers. As the SoC architectures become increasingly complex, NoC architectures can make chip design easier and allow optimized connection topologies. The founders were Alain Fanet, César Douady and Philippe Boucard, with a joint history first at Matra and then as founders of T.Sqware. T.Sqware was sold to GlobespanVirata for over USD 200 million in 2000.

The company moved its headquarters to San José in 2007. It had about 26 employees in Paris and 8 in San José.

Arteris is a venture-capital backed start-up. Its first-round investors included the Palo Alto -based Crescendo Ventures, Munich-based TVM, and French Ventech, and Atlas Venture. It raised over USD 12 million in the first round of investment in 2003, and received 1.5 million euro interest-free loan from Anvar, the French agency that operates under the aegis of the Ministries of Industry, SMEs and Research. The second round of investments was led by the current EDA leader Synopsys, raising USD 8.1 million in 2007. The third round was led by the Japanese DoCoMo Capital in 2008, raising USD 7.5 million. According to the Arteris press announcement, this brings the total investment in the company to USD 25 million, with more than USD 32 million in equity funding from an international set of investors.

Arteris introduced it first product in March 2005. This was globally the first commercial implementation of a Network-on-Chip. The NoCSolution consists of NoCexplorer that can be used to design the network on chip, and NoCcompiler that creates the actual logic that is implemented on the chip to connects its various IP blocks. The product is available on either per project license or royalty pricing models. When the product was first introduced, the pricing was announced to start at USD 350,000. Its customers include STMicroelectronics, Texas Instruments, Thales, and NEC.

In 2007, Arteris had product sales of 113,000 € and service sales of 360,000 €, and its operating income included 2.133 million € assets produced in-house. The operating income was – 4.884 million Euros and its profit was -4.5 million Euros.

Patriot Scientific Corporation

Patriot Scientific was founded in 1987 with technologies applicable for U.S. Department of Defence applications. In 1994, the company developed a 32-bit microprocessor architecture and in 2001 it began licensing its microprocessor chip as an IP core.

Patriot Scientific evolved in 2005 into a IPR holding company, unifying its patent portfolio with the TPL group, which focuses on IPR management services, including the maximization of cash return of IPR portfolios. The Patriot Scientific patents are commercialized by Alliacence, a TPL Group enterprise, which according to its own description employs a cadre of IP-licensing strategists. TPL and Patriot assert that their jointly owned patents protect techniques used in almost all microprocessors, microcontrollers, digital signal processors, embedded processors, and SoC implementations. Patriot and TPL believe that at least three of their patents are elemental to virtually every microprocessor design. These include:

- U.S. 5,809,336: Clocking CPU and I/O Separately
- U.S. 6,598,148: Use of Multiple Cores and Embedded Memory
- U.S. 5,784,584: Multiple Instruction Fetch.

The patents were granted in 1998 and they are valid through 2015. The Patriot patent portfolio is licensed by Intel, AMD, HP, Casio, Fujitsu, Sony, Nikon, Olympus, Kenwood, and Nokia, among others.

A purely IP-based firm, which licenses IP designs and also heavily relies on patent licensing, is Rambus, based in Los Altos, California. The total revenues of Rambus were 180 million USD in 2007. It gains the majority of its revenues by licensing its broad portfolio of memory interface patents to semiconductor and systems companies. These licenses are royalty-bearing. In 2007, the three largest licensees, AMD, Fujitsu and Qimonda, generated royalty revenues of about 72 million USD. Rambus, however, also extensively sells its design IP. These "product licenses" typically include one-time fixed-cost components and ongoing license fees. As the integration of Rambus technologies often require detailed knowledge on the provided IP, the contracts also usually include a fixed cost engineering component. For Rambus, these engineering contract revenues were about 14 percent of total revenues in 2007. Royalty revenues, which include patent royalties and IP license fees, were 154.3 million USD in the same year.

A somewhat special characteristic of Rambus is that a large fraction of its royalty revenues has been created through litigation. Rambus had over 680 patents and about 540 patent applications at the end of 2007, and it claims to hold valid patents for some key memory technologies, including synchronous dynamic random access memories (SDRAM) and double data-rate (DDR) memory interfaces. These technologies are critically important in many digital devices and related Rambus IP rights have been contested by major semiconductor manufacturers. During the last years, the patent litigation expenses of Rambus have been close to 40 million USD, annually.

New business models are currently emerging that aim to commercialize captive semiconductor IP that until now has been difficult to utilize. For example, IPextreme, Inc., based in Campbell, California, provides standardized license agreements that allow third parties to access IP from major semiconductor firms. The IP can be downloaded from the IPextreme's web portal. A similar service was launched in February 2008 by Think Silicon Ltd., a design service and IP core provider, based in Patras, Greece. Its IP Partnership programme is aimed towards companies and contractors who have developed IP cores for internal use, but are unable or unwilling to sell and support their designs in the market. Think Silicon works closely with those companies to allow them to commercialize their designs by utilizing its IPGenius platform and providing them with live usage status. The IPs are obtained in source code form with simple licensing terms and delivered to users through a web portal. IPextreme is further detailed in the box below.

IP Aggregators

IPextreme is an example of IP aggregator that focuses on commercializing captive IP from large semiconductor and systems firms. IPextreme now provides access to IP from Freescale, Infineon, Cypress, National Semiconductor, NXP, and Mentor Graphics. Its online marketplace, the Core Store, offers IP to all interested parties for a fixed price, without having to conduct further negotiations or work through middlemen.

Freescale Semiconductor was among the first IPextreme's Core Store partners, making its ColdFire V1 32-bit processor core available for licensing through the Core Store in January 2008. For a fixed rate of $10,000 per single user, systems designers will be able to license and download the ColdFire V1 code in encrypted Verilog format, plus documentation and integration testbech and tests. According to Freescale, such IP would typically made available to the market at $100,000 to $300,000. Freescale is providing its IP through IPextreme in an attempt to attract new cost-conscious users for its IP.

At present, also National Semiconductor provides fixed-price IP through Core Store. For example, one can download a smart card interface from National Semiconductor for 2,000 USD.

A major problem with the independent IP model is the need to negotiate licensing contracts. As complex SoCs can include dozens of IP blocks, the legal effort easily overwhelms the technical complexity of integrating IP blocks from different vendors. This challenge is specifically addressed by services such as the SignOnce Program supported by Xilinx, the leading provider of FPGA chips. Since 2001, the SignOnce IP licenses have been used to provide common license terms for FPGA-based soft IP. Users of IP therefore do not have to negotiate separate licenses for third-party IP. Instead, they can use a standardized contract to access all the IP provided by the partners in the SignOnce Program. In June 2008, there were 476 cores available through SignOnce.

Large electronics manufacturers have also created spin-offs to commercialize their semiconductor IP. For example, in April 2007, Philips spun-off Silicon Hive B.V., as an independent IP supplier. Silicon Hive, headquartered in Eindhoven, has developed a fast media processing architecture, which it sells to semiconductor and consumer electronics industry, targeting communications, video, and image applications. Silicon Hive also sells software development tools that support the development of systems that use its IP cores. The company employs now about 50 people.

Many fabless semiconductor firms both use their IP internally to develop chips and also license it to other system developers. For example, Silicon Image, Inc., based in Sunnyvale, California, is one of the leading providers of digital video cores. It uses IP licensing as a complementary revenue stream for its product sales, as well as to facilitate the adoption of technologies where it has intellectual property rights. Most of the IP it licenses has field of use restrictions that prevent the licensee from building chips that compete directly with Silicon Image's products. In fiscal 2007, Silicon Image had total revenues of about 320 million USD. Licensing, royalties and related development work generated 16 percent, or 50.8 million of the total. In 2006, the revenues form licensing, royalties and related development work were 44.6 million, including about 12 million of royalty revenues originating from a settlement agreement with Genesis Microchip. Its IP licensing agreements generally include a nonexclusive license for the underlying IP. Fees under these agreements typically include license fees, maintenance and support, and royalties payable following the sale of products incorporating the licensed technology.

5.3.1 Top 20 IP Core Vendors

The largest IP vendors are listed in Table 7 below. The table shows revenues generated from licensing IP, excluding one-time legal settlement fees. For year 2007, the table shows revenues for each company from its fiscal year ending in 2007. As the fiscal years end in different months for different firms, the numbers do not exactly correspond to the industry revenues in year 2007. TTPcom, based in Melbourne, UK, and a leading supplier of wireless IP in the early years of the decade, was acquired in 2006 by Motorola. Its numbers are estimated from its last registered annual report, for a period ending 31 December 2006.[78] Data for privately-owned US firms is based on estimates, where a number of data sources are used. For Tensilica, Inc., we use unverifiable data from its web site, giving the employee count of 120. The 2007 revenues for Tensilica are estimated at USD 30 million, based on market studies from earlier years and company news reports. This is considerably more than the sales estimate by Hoover's, at the USD 9 million. Tensilica is a privately owned company based in Santa Clara that focuses on configurable and synthesizable

78 The 9 month period ending in 31 December 2006 shows third-party contract revenues of £25 million and licensing to Motorola for £7.9 million. In addition, it shows R&D services to Motorola worth of £21.5 million. The average number of employees for the year ending March 2006 was 464, and for the nine month period ending 31 December 2006 it was 375. We use assume that the employee count declined linearly after the acquisition to arrive a year end count of 286 employees.

Table 7: Top 20 IP vendor revenues and average employee counts, 2007

Rank 2006	Rank 2007	Company	Employees 2007	IP Revenue ($M) 2007	2006	2005	Growth 07/06	2007	Cumulative
1	1	ARM	1728	516	484	419	6,6%	29,2%	29,2%
2	2	Rambus	430	180	194	157	-7,4%	10,2%	39,4%
3	3	Synopsys	5 196	97	91	74	6,6%	5,5%	44,9%
7	4	Motorola-TTPcom*	286	87	43	53	102,0%	4,9%	49,8%
4	5	MIPS	196	83	76	59	9,2%	4,7%	54,5%
6	6	Mosaid	112	57	54	40	5,9%	3,2%	57,8%
10	7	Silicon Image	635	51	33	19	54,9%	2,9%	60,7%
5	8	Virage Locic	417	47	57	51	-18,4%	2,6	63,3
8	9	Imagination Technologies	366	43	39	29	11,2%	2,4%	65,7%
9	10	SST	715	40	37	37	7,6%	2,3	68,0%
11	11	CEVA	192	33	33	36	2,2%	1,9%	69,9%
12	12	Chipidea	310	33	32	25	3,1%	1,9%	71,7%
13	13	Tensilica*	120	30	27	20	11,1%	1,7%	73,4%
14	14	ARC	196	29	25	19	15,6%	1,6%	73,4%
15	15	Mentor Graphics	4 358	25	25	23	0,0%	1,4%	74,8%
16	16	Wipro-Newlogic	350	21	19	14	10,5%	1,2%	76,0%
19	17	Dolphin Integration	164	17	13	13	30,0%	1,0%	76,9%
17	18	Mosys	184	14	15	12	-4,7%	0,8%	77,7%
18	19	Analog Bits*	N/A	13	13	11	0,0%	0,7%	78,5%
20	20	sci-worx	172	-	12	9	-	0,0%	78,5%
		Others		*350*	220	204	59,1%	19,8%	100,0%
		Total		1 766	1 542	1 323	14,5%	100,0%	

Source: Author´s calculations based on company reports; iSuppli, 2007.

digital signal processing cores. It has over 120 licensees, including AMD, Broadcom, Fujitsu, Intel and STMicroelectronics. Similarly, accurate data for the privately-owned Analog Bits, Inc., is not available. As a reference for earlier years, we use data provided by iSuppli.[79]

Rankings provided by market research firms are very popular among vendors as the top positions are useful for marketing. The reality behind the rankings, however, is complex as the firms have very different revenue stream structures. The rankings of IP vendors also changed considerably during 2007 due to a number of mergers and business re-orientations. Silicon Image acquired the German sci-worx, previously a fully-owned subsidiary of Infineon, in January 2007. In Table 7 the revenues from sci-worx for 2007 are included in Silicon Image's revenues. Mosaid sold its semiconductor IP product business to Synopsys for 15.3 million USD in June 2007. Mosaid now focuses on patent licensing. Lisbon-based Chipidea, the leading supplier of analog and mixed-signal IP cores, was acquired by MIPS Technologies in August 2007, and is now called MIPS Technologies Analog Business Group. When IP revenues have not been included in the fiscal year revenues for the acquiring company, the table shows entries for both.

In 2008, the list of top 20 IP vendors continues to change. At the beginning of 2008, Motorola effectively closed down TTPcom, when it announced redundancies for about 155 of its employees.

In June 2008, Cadence Design Systems Inc., the leading EDA vendor made a hostile bid for the third largest EDA vendor Mentor Graphics Inc., for USD 1.6 billion. The bid didn't go through, and subsequently Cadence fired its CEO and landed in the midst of an accounting scandal as the firm had overstated its revenues by booking possible future income as revenues. Historically,

79 The revenues estimated by iSuppli are different but roughly consistent with estimates from Gartner/Dataquest. However, for TTPCom the Gartner numbers are almost double. The iSuppli estimate looks very low. One potential source of discrepancy is that iSuppli uses GBP numbers for TTPCom, instead of USD.

Cadence has tried to avoid competing with independent IP vendors that create IP for the users of Cadence tools. Mentor appears on the table above, as it also creates substantial revenue streams from IP licensing.

Focusing on revenues easily misses important aspects of the IP core ecology. New start-up firms typically do not create revenues for several years. When they do, they are often acquired by existing firms. The innovation and revenue creation models are also changing today. As many open source projects have shown, it is possible to develop high-quality technical systems outside business firms. Although the economic impact may be large, these initiatives are almost invisible in economic indicators. The open source model is rapidly gaining popularity also in the semiconductor IP field. The box below highlights some developments in open source semiconductor IP.

Will Open Cores Revolutionize the IP Industry?

Several open source software projects have proved the viability of self-organized distributed innovation and development models that rely on networked communications and content sharing. During the last decade, it has often been suggested that this development model could successfully be used beyond software development. For example, von Hippel (2005) states that there exists a clear analogy between innovation communities that develop sports equipment and open source software innovation communities. Rarely, however, innovation researchers have discussed in detail the requirements that make the open source model possible and successful. It therefore remains unclear whether the open source innovation model actually can be applied in other domains, for example, in innovative design and engineering of physical products such as semiconductor devices.

One success factor in open source software projects has been the fact that software is both the description of a system and the system (Tuomi, 2002a). In almost all other technical domains, descriptions are only abstract representations of the system. This has important consequences for the underlying innovation dynamics, in particular, when the innovation process is distributed.

Several initiatives exist today that try to extend the open source development model to IP cores. These include the OpenCores initiative, which acts as a portal for a large number of open core projects, OpenSPARC, which, for example, provides the source code for Sun's UltraSPARC processors, and the GRLIB IP core architecture from Geisler Research, which includes, for example, the GNU GPL licensed definitions of the configurable LEON3 processor and in-chip bus controllers.

Although, for example, OpenCores claims that more than a million engineers from more than 10,000 organizations world wide have downloaded IP from OpenCores in the first 8 years of its existence, there is no accurate data on the viability of the open hardware model. As IP cores are implemented as physical systems, their designs and implementations are distinct. This is one of the reasons why the verification costs of IP cores is rapidly increasing when the complexity of cores increases and the feature sizes decreases.

Yet, as the history of the Linux operating system kernel shows, technical development can be very fast if a "core kernel" can be stabilized so that peripheral innovation becomes possible. Such development dynamics require standardized interfaces and a relatively stable "core" that provides a shared foundation for measuring progress and comparing alternative designs. If semiconductor IP architectures have such a central core, they may have innovation dynamics that resemble open source software.

A preliminary statistical analysis of open IP core projects, conducted in parallel to the present study, indicates that IP core projects are different from typical open source software projects. With appropriate enablers and infrastructure, open source semiconductor IP could become highly important for future developments in ICT.

5.3.2. The Geographic Dimension

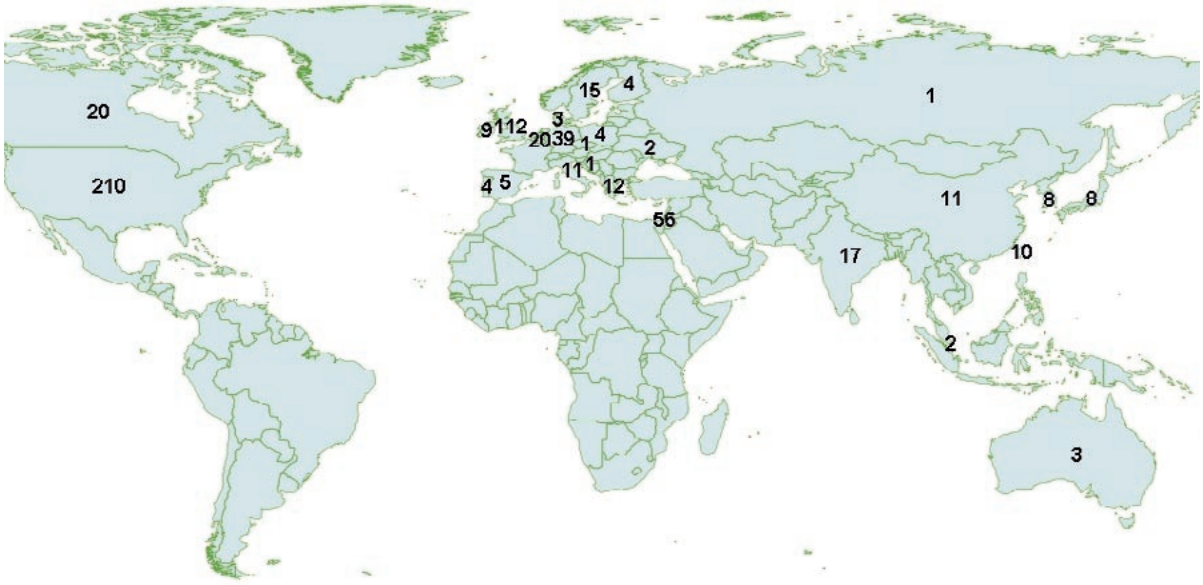
As noted above, historically the semiconductor industry has been a leader in globalization. The offshoring of semiconductor production started already in 1961 when Fairchild launched its first assembly plant in Hong Kong. From this beginning, the industry rapidly diffused to other East Asian locations, forming a complex network of production activities. A key driver in this geographic expansion was the availability of cheap labour. Gradually, however, knowledge and availability of technical skills have become increasingly important. Today, semiconductor industry consist of a geographically differentiated system of production where knowledge and production activities concentrate in a small number of global hubs.

The semiconductor IP and design activities represent the most knowledge intensive part of this value system. Although IP firms tend to locate close to the major hubs of semiconductor industry, when the industry becomes globally networked it is not possible anymore to be close to the centre. Even the smallest IP firms have to be globally networked to be successful. Yet, many small IP firms are also geographically concentrated and rely on locational advantages. A major driver is the location of university and industry research centres, from which many IP start-ups have spun off. Similarly, small IP firms often have succeeded because of a close proximity and tight social networks with a major customer. In Europe, the key customers have included the large telecommunications and consumer electronics manufacturing firms, and, for example, aerospace, car, and industrial automation enterprises.

To study the geographic dimension, we used a proprietary dataset of 682 semiconductor design and IP firms. The firms in the data set consist of businesses that actively market design IP products, as well as European fabless semiconductor firms and design houses. In addition, the next chapter will analyze in more detail developments in China.

Using the dataset, a rather clear picture emerges. Of these firms, 210, or 31 percent are headquartered in the US. In Europe, the UK is clearly the largest host country of design and IP vendor firms. Israel also has a very strong concentration of semiconductor design and IP

Figure 12: Geographic distribution of semiconductor IP creators



Source: Meaning Processing, 2008.

vendor firms, with 54 firms. The distribution of these firms in different countries is shown in Figure 12. The relatively low count of firms in China and India in the figure reflects the fact that only few Chinese and Indian firms market their IP globally. As was noted in the section on India, there are about 130,000 people working in electronics design services in India, and about 17,000 of these work in VLSI design industry. This is slightly more than the total employment in the top 20 IP vendors. Over half of the Indian ICT design employment, however, is in multinational firms and a large majority of the rest is in captive units of Indian design service firms. Only few Indian firms, therefore, market their IP as independent products. Similarly, although China has over 500 semiconductor design firms, as discussed in the next chapter, only few of these market their IP. In addition, some Chinese IP firms have set up their headquarters in Silicon Valley, where international customers are easy to access.

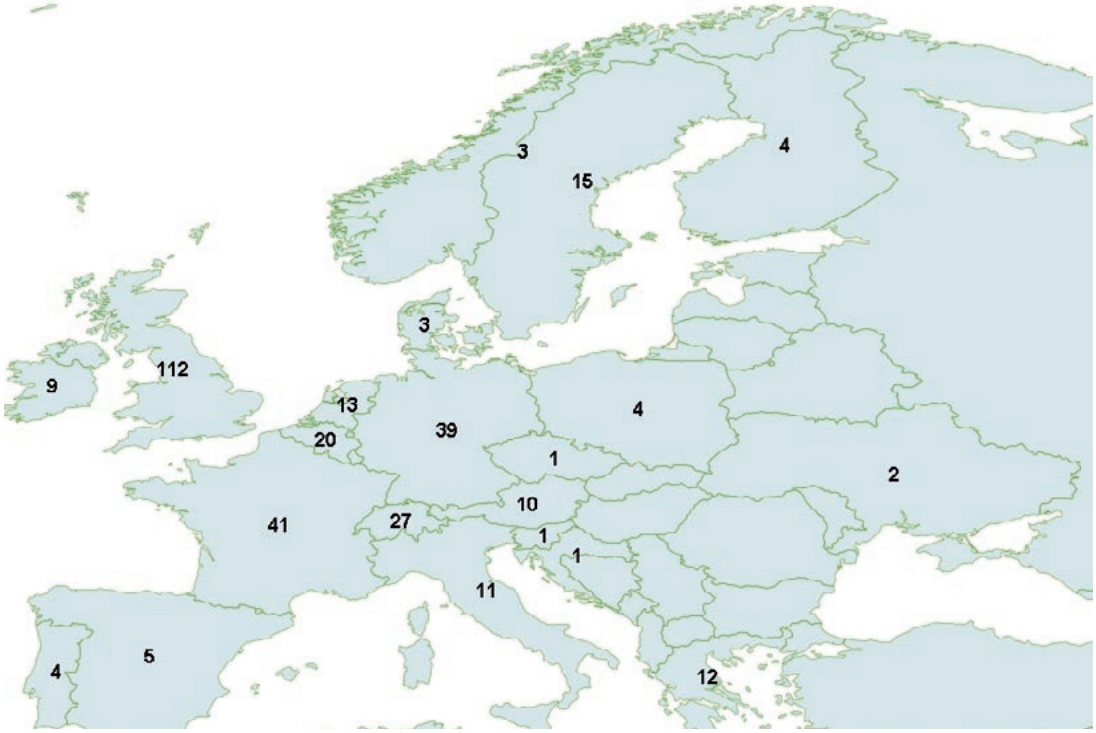
The geographic concentration of IP vendors becomes clearly visible when the headquarter address locations are shown on the map. This can be seen in Figure 13, which shows markers for firms headquartered in the US. As can be seen from a close-up on the San Francisco Bay area on top of the map, Silicon Valley has a very considerable concentration of firms specializing in this domain, with almost one hundred firms within a 20 kilometre distance from the centre of Mountain View.

Focusing on Europe, the UK, France, and Germany emerge as the countries with the highest number of firms. This can be seen in Figure 14.

Figure 13: Semiconductor IP vendors in the US.

Source: Meaning Processing, 2008.

Figure 14: Fabless semiconductor firms, design houses, and IP vendors in Europe.

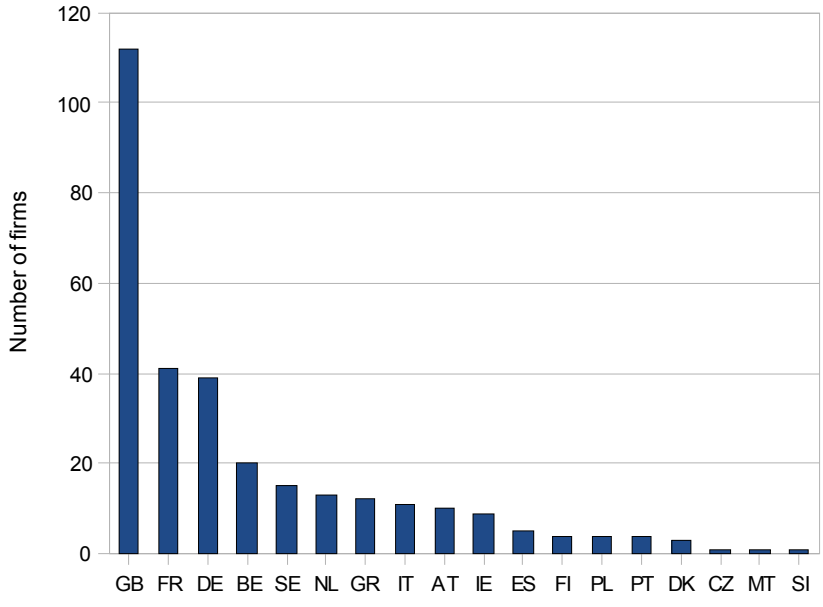


Source: Meaning Processing, 2008.

For the EU27 countries, the distribution of fabless semiconductor firms, semiconductor design firms, and IP vendor firms is shown in Figure 15. The total number of these firms is 305.

Not all these firms market their semiconductor IP, as the data shown in the figure also include fabless firms and design houses that use their IP only internally. The data include firms that have

Figure 15: Fabless semiconductor firms, design houses and IP vendors headquartered in EU27, year 2008.



Source: Meaning Processing, 2008.

their headquarters in EU27 or which otherwise are known to have roots there. As the graph shows only the number of firms, the actual number of establishments is much larger. The full list of establishments would include, for example, subsidiaries in other EU27 countries, and also establishments of firms headquartered outside EU27. Although an establishment level analysis would be useful for mapping the actual design competences in Europe, we have not done this in the present study.

A small number of European and Asian firms have moved their headquarters to the US, mainly to Silicon Valley, at the same time retaining the majority of their activities in their original locations. Similarly, some European firms have been acquired by firms based in the US and India, while still maintaining the European firms as relatively independent subsidiaries. To the extent that the real locus of activities remains in Europe, the numbers above have been adjusted. For example, Wipro-Newlogic, now fully owned by the Indian Wipro, is counted as an Austrian firm, as its main locus of activity is in Austria. Similarly, the graph also counts Hantro Oy, which develops video coding IP for wireless telecommunications and Bitboys Oy, as a Finnish IP firms, although they are now owned by On2, headquartered in New York and Qualcomm, headquartered in San

Where are the Bitboys?

Bitboys Oy was founded in 1991 by two young computer hackers Mika and Kaj Tuomi. The firm was based in Noormarkku, a community of about 6,000 inhabitants on the west coast of Finland. The closest city is Pori, with about 80,000 inhabitants.

The firm was set up to develop computer graphics that was in high demand in the demo scene. In the demo scene computer enthusiasts competed in trying to create impressive audio and graphics programs, often for the Commodore 64 and Amiga microcomputers. Originally, the demos were short inserts that computer crackers added to programs while circumventing their copy protections, but the development of independent demos started to gain popularity in towards the end of 1980s. Since 1992, the Finnish demo scene was organized around the internationally well-known Assembly meetings that has gathered thousands of computer hobbyists to its annual programming parties.

At first, Bitboys tried to develop its own graphics chips. This became difficult as the competition increased rapidly in the 1990s. Fabs also declined to make chips for the firm as it was too small and risky. In 2002, Bitboys focused on video IP for mobile phones, leaving the PC graphics business.

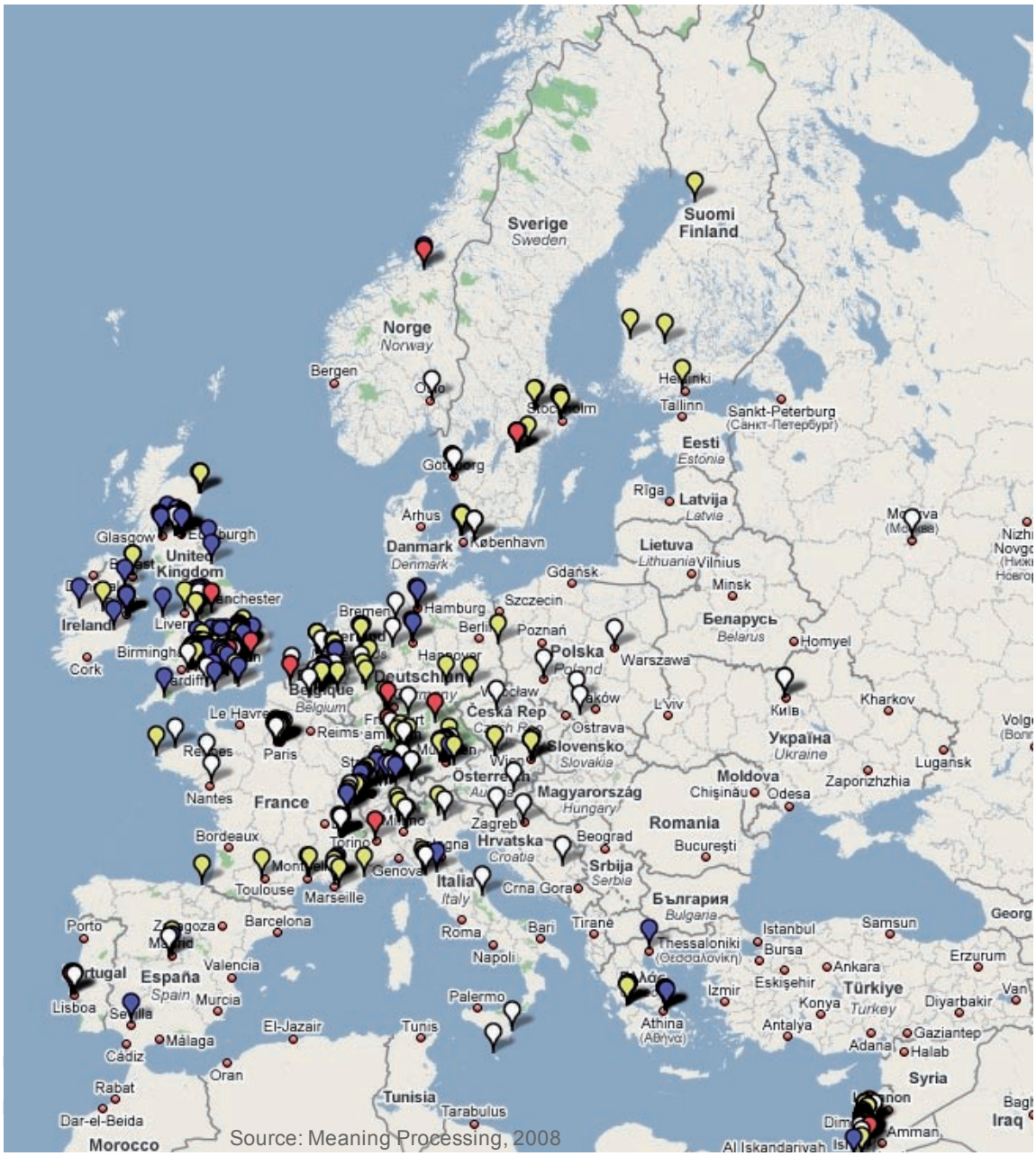
In 2006, Nokia indirectly revealed that it is a customer of Bitboys and that it had earlier invested about four million Euros to the company. Soon after, the fabless graphics chip firm ATI bought Bitboys, paying 35 million Euros for the firm that had revenues of about 5 million and 45 employees. The CEO of Bitboys became responsible for ATI's mobile phone graphics division. The firm changed its name to AMD Finland a couple of months later, when the processor maker AMD bought ATI. In January 2009, AMD Finland was sold to Qualcomm for 50 million in cash. The firm has now 50 employees in Noormarkku and Espoo. The firm has licensed its IP cores to most mobile phone makers and many mobile chip makers. In analyzing the geographic distribution of firms, we count the firm as a Finnish IP firm.

An important design criteria for mobile phone processors is small die space and low power consumption. In contrast to desktop PCs, where both processing power and electricity is abundant, the technical limitations of mobile phone platforms resemble the constraints of a Commodore 64. Demo programmers have, therefore, been well equipped to program and design mobile phones.

The founders are now in their late 30s. CEO Mikko Saari, a childhood friend of the founders, noted in an interview in 2007:

> "University education is still light years behind the leading edge. We, and firms like us, are the real university."

Figure 16: Locations of chipless firms in Europe.



Source: Meaning Processing, 2008.

Diego, respectively. In addition to the numbers shown above, there are many regional offices and R&D centres of international firms in Europe. These are not included in the data above. As the population of firms is a dynamic one, the numbers change continuously., and the data above represents the situation in July 2008.[80]

80 For example, we include Gaisler Research AB in EU27. It was recently acquired by Aeroflex Incorporated, based in the US. Similarly, we count as an Austrian firm the NewLogic, which is now fully owned by Wipro, and which also has a subsidiaries in France and Germany.

The dataset contains 271 firms located in EU27, Norway and Switzerland, and 56 firms located in Israel. In EU27, Norway and Switzerland, over 150 firms actively market their IP cores. The locations of these pure-play IP firms are shown in the picture below.

The UK is clearly the leading EU country when the number of semiconductor firms is counted. Partly this is because of historical reasons, related to the early expansion of IDMs to low cost regions such as Scotland. We detail the historical developments that have led to the strong concentration of semiconductor activities in Table 8.

In the top 20 IP vendor list, the nine firms shown in Table 8 have the locus of their activities and roots in Europe. Four of the firms actually still have their headquarters in Europe; the rest have recently been acquired by non-European firms.

As noted in Table 8, TTPCom was acquired by Motorola in 2006, and its operations were considerably scaled down in 2008. At present, it is not known whether TTPcom will have any IP activities in 2009. CEVA is currently headquartered in Silicon Valley. It was formed by merging the IP businesses of Parthus Technologies plc, located in Ireland, and DSP Group, headquartered in Silicon Valley but with roots and heavy presence in Israel, in 2006. The Silicon Valley based MIPS acquired ChipIdea in 2007. Chipidea, founded in 1997 by three university professors from the Technical University of Lisbon, is now the Analog Business Group of MIPS Technologies. It has

The Story of UK Semiconductor Industry

Today there are over 110 semiconductor design firms in the UK, making it the clear leader in the EU. This set of firms includes both fabless firms, such as Cambridge Silicon Radio, Wolfson Microelectronics, and XMOS, and firms such as the chipless IP market leaders ARM, Imagination Technologies, and ARC International. Design firms are concentrated around three main geographical locations: Silicon Fen (Cambridge), Silicon Glen (Scotland), and Silicon Gorge (Bristol).

The reasons for the large number of design firms in the UK deserve further study. Some key factors, however, are well known.

Since the 1960s, Scotland was the preferred location for the US semiconductor firms that wanted to access the EEC and the British defence market. The fact that a 17 percent EEC tariff was levied on the value added during the production process, meant that firms such as Motorola and National Semiconductor set up high-value adding fabs in Scotland, shipped the wafers to East Asia for assembly and testing, and then imported the products back to Europe. Scotland was an attractive location partly because skilled workers were available at low cost, and as the universities in the area were able to produce skilled workers at adequate quantities. According to Henderson (1989: 129), semiconductor firms were also able to circumvent labour conflicts with less-skilled workers by recruiting young women, resisting unionization, adopting new bonus systems, and by locating their plants in new industrial areas. The activities of various central and local state agencies and government subsidies also played a role. By 1983, Scotland produced 79 percent of British and 21 percent of European integrated circuits. The emergence of a local production complex with complementary capabilities has further strengthened the position of Scotland as a regional hub in the semiconductor industry.

Future Horizons argues that one reason for the large number of UK design firms is the massive streamlining, restructuring and privatization of electronics firms since the 1970s, which released large numbers of skilled managers and researchers to set up their own firms. The earlier exodus of British engineers to the US had also created a substantial pool of expatriates who understood business. Combined with cuts in defence spending, semiconductor designers had to find new competitive business models. The role of government initiatives and national champions, including INMOS and GEC-Plessey, as well as innovative entrepreneurs, such as Clive Sinclair and Herman Hauser, have also been important.

Table 8: Top 20 IP firms with locus of activity in Europe.

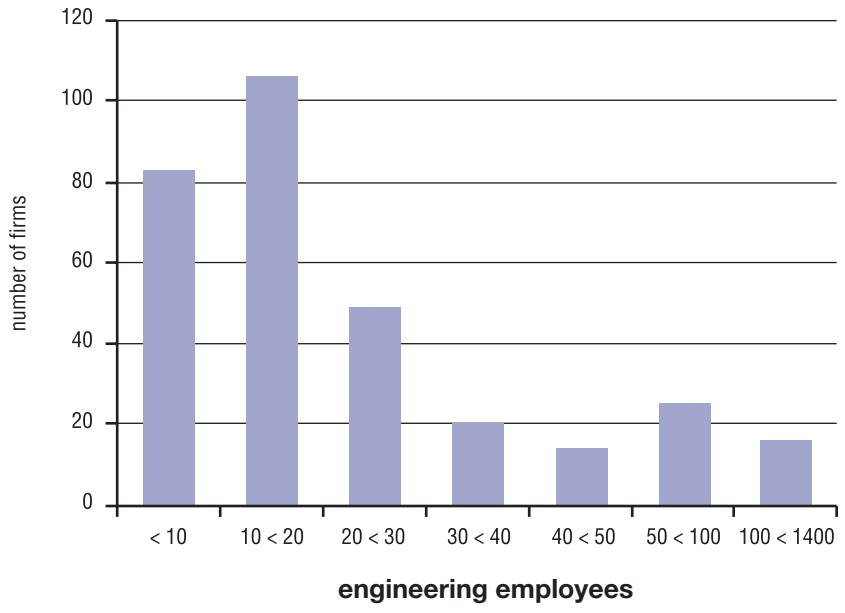
Rank		Employees	IP Revenue ($M)
2007	**Company**	**2007**	**2007**
1	ARM	1728	516
4	Motorola-TTPcom	*286*	*87*
9	Imagination Technologies	366	43
11	CEVA (Parthus, DSP Group)	192	33
12	MIPS Analogue Group (Chipidea)	310	33
14	ARC	196	29
16	Wipro-Newlogic	350	*21*
17	Dolphin Integration	164	17
20	sci-worx (now part of Silicon Image)	172	-
	Others	*1000*	*150*
	Total EU (est.)	4764	929

Source: Meaning Processing, 2008.

engineering centres in Portugal, France, Belgium, Poland Macau and China. ARC International, in turn, is still firmly based in Saint Albans, UK. NewLogic, based in Austria, has been fully owned by the Indian Wipro since 2005. Dolphin Integration is based in Meylan, France, and it has offices also in Germany and Canada. Sci-worx has been headquartered in Hannover, Germany. In 2007 it was acquired by Silicon Image, Inc., based in Silicon Valley.

Table 8 also gives the average number of employees in the top ranking IP firms and adds a rough estimate of the employer count in other

Figure 17: Number of engineers employed by European semiconductor design and IP firms.



Source: Author's calculation based on data from Future Horizons, 2007

smaller European IP firms. It should be noted that the European IP firms employ an increasing number of people outside Europe, and that the estimated number does not include captive design activities or most research and design units owned by firms headquartered outside Europe. The employee counts, therefore, do not map in any direct way to employment in Europe.

Figure 17 shows the number of different sizes of European fabless, chipless and design firms, based on the number of design engineers they employ. The data comes from Future Horizons, 2007, and it includes a subset of firms that we used above. The actual number of employed persons is considerably higher, as the Future Horizons data only include engineers, and as it also in some cases seems to count engineers based on somewhat outdated data. The data, however, gives a good picture of the distribution of the firm sizes.

In the next section, we describe in more detail the Swedish IP vendors, including their worker compensation.

5.4 An In-Depth Look at Swedish IP Vendors

In the present study, we analyzed in detail Swedish semiconductor IP vendors to get a close-up view on the smaller firms engaged in the area. In general, it is difficult to know what these firms are doing, as most of them are small private firms, and as media reports on them are not always completely accurate. We therefore first collected data on all semiconductor activities in Sweden, located firms that market their products and services to outside customers, and analyzed the annual financial reports of those firms that market IP cores. In Sweden, business firms are required to file annually their financial records, and these are available through the public registrar.[81]

Sweden has over 80 firms that in recent years have been engaged in semiconductor design activities. Many of the larger ones are design departments in diversified global companies. LM Ericsson is the historically most important of these, but, for example, ABB, Cambridge Silicon Radio, Catena, Flextronics, Huawei, Infineon, Nokia, Saab and Zarlink all have had semiconductor research and design centres in Sweden. Several reorganizations have changed the company landscape in recent years, however. For example, Ericsson Microelectronics was acquired by Infineon in 2002. The chip fab in Kista was shut down in August 2004, and the R&D activities were moved to Germany and Asia in 2007. At that time the Infineon offices in Linköping were taken over by Signal Processing Devices AB, which also hired most of the designers.

In our dataset, we have 16 semiconductor design and IP vendor firms that have their headquarters in Sweden, and which actively market their services to outside customers. Nine of these license semiconductor IP cores. One is Mocean Labs, which focuses on car entertainment systems, and which provides a Media Oriented Systems Transport (MOST) controller for Xilinx FPGA chips. There is no data available on the revenues from this product, and we therefore have excluded Mocean from a more detailed analysis.

The eight companies that can be categorized as IP core vendors are listed in Table 9. The data is from the last financial report registered by June 2008.[82] The currency is converted from SEK to

81 Although small firms do not have to state their financial reports using international accounting practices, Swedish reporting practices are well developed and to some extent more detailed than in other countries. For example, Swedish companies normally report the number of male and female employees, worker absence rates, and management compensation in detail. The reports are available in Swedish.

82 As some of the firms have financial periods that end mid-year, the most recent available report is for fiscal 2006.

Table 9: Swedish IP vendors, revenues, profits, and employment.

Name	Founded	Financial Year	Revenues (12 mo.)	Profit (12 mo.)	Employees	Personnel Costs	Total Assets	Personnel cost per employee
BitSim AB	2004	2006	4793	76	37	3014	1221	81
Gaisler Research	2001	2007	2370	1154	11	786	1380	71
Logipard AB.	2000	2007	1282	62	10	586	1778	59
Wavebreaker AB	2004	2007	691	-607	15	945	255	63
InformAsic AB	2004	2006	531	23	5	381	184	76
SP Devices	2001	2007	529	-742	15	975	1428	65
RealFast	2001	2006	463	-41	4	491	372	123
Coresonic	2006	2007	0	-280	2	165	305	82
Total			10660	-356	99	7343	6924	

Source: Author´s calculations based on company reports

euro from 31.12.2007, and given in thousands of Euros. [83] As some of the firms have reported periods that are over 12 months, the revenue numbers are for a 12 month period. The table also shows average annual employee counts.

Measured in terms of revenue and employees, BitSim AB is the largest Swedish IP vendor. Most of its revenues, however, come from design and consulting activities. The second largest is Gaisler Research, which specializes in configurable IP cores used in demanding environments such as aerospace. The third largest vendor is Logipard. It specializes in video coding and image processing. Its core design team originated in C-Technologies, moved to Anoto AB, and was spun-off from Anoto in December 2006. The fourth is Wavebreaker, which is currently part of Flextronics. Wavebreaker focused on wireless technologies. The fifth is InformAsic. It mainly does customer development projects for FPGA and ASIC chips. It also sells IP cores for security and encryption applications. A relatively rapidly growing IP vendor is Signal Processing Devices AB (SP Devices). It focuses on signal processing software and IP cores for telecom, medical technologies, and measurement. In 2007, SP Devices received venture funding of about 3 million Euros from SEB Venture Capital. SP Devices took over the offices and hired designers from Infineon when Infineon closed down its office in Linköping. At the end of 2007, SP Devices had about 20 employees. RealFast (RFHC RealFast Hardware Consulting AB) has not yet filed its report for the fiscal 2007. It is single person owned firm that seems now to be focusing mainly on education.[84] Coresonic, in turn, is a start-up that develops its LeoCore processor architecture for wireless and digital television applications. At the end of 2006, Coresonic had four employees.

5.4.1. Description of the Swedish IP Vendors

A description of the firms is shown on the next page. The table shows average employee counts and key financial data for the last available year.

83 Using exchange rate 0.1059 €/SEK.

84 The web site for RFHC RealFast Harware Consulting AB is maintained by RFE RealFast Education AB. In ChipEstimate its cores are listed under Real Fast with a P.O.Box address in Colorado. In Xilinx SignOnce licensing partner list, it is listed as RealFastOperating Systems AB, which links to Prevas AB, which is registered as the vendor for RealFast Sierra16 Operating System Accelerator. RealFastOperating Systems AB does not exist in the Swedish registers.

BitSim AB				
Employees: 37	Personnel costs: SEK 28,461,063	Revenue: SEK 45,259,024	Operating Profit: SEK 714,142	Assets: SEK 11,530,171
Data from year 2007	Founded 2000			

BitSim is an independent design house specializing in FPGA and ASIC designs. It also sells its BADGE IP core 2D graphics accelerator that can be embedded in FPGA or ASIC designs. The firm is based in Sweden in several locations and offers a broad range of services from a design consultation to undertaking of an entire project. BitSim also offers design of circuit boards and complete systems. BitSim also outsources its projects to external consultants (materials and outsourcing were 12 million SEK in 2007; personnel costs were 28 million). During 2001 BitSim became a qualified consultant partner with Altera and Xilinx. The initial end markets Telecom and Industrial expanded during 2005 into Defence and Medtech. During 2006, BitSim expanded with new offices in Lund (Southern part of Sweden), Gothenburg (Western region) and Uppsala (North of Stockholm). During the fall of 2006 BitSim started an educational service offering, BitSim Education.
At the end of 2007, BitSim had 43 employees, a growth of 42 per cent from the previous year. It opened offices in Göteborg and Uppsala. It licensed the first ASIC version of its BADGE graphics core. New customers included Ericsson in Göteborg, Elektrobit, Sustinere, VSYSTEMS, Host Mobility and Scheider.

Coresonic				
Employees: 2	Personnel costs: SEK 1,554,257	Revenue: SEK 0	Operating Profit: SEK -2,647,053	Assets: SEK 2,881,831
Data from year 2006	Founded 2004			

Coresonic AB is a privately owned Swedish company developing and marketing semiconductor intellectual property for baseband processor technology. Coresonic has developed a novel, patent pending, processor architecture enabling flexible multimode communication applications at low cost and low power consumption. The technology is suited for all types of mobile wireless devices from mobile phones and PDAs to wireless networking and digital broadcasting. The company was founded in 2004 to commercialize a programmable baseband processor technology from a research project at Linköping University, led by Prof. Dake Liu. Coresonic's main office is in Linköping, Sweden.

Gaisler Research				
Employees: 11	Personnel costs: SEK 7,423,677	Revenue: SEK 22,383,923	Operating Profit: SEK 10,900,315	Assets: SEK 13,028,686
Data from year 2007	Founded 2001			

Gaisler Research AB, based in Gothenburg, provides IP cores and supporting development tools for embedded processors based on the SPARC architecture. The key product is the LEON synthesizable processor model together with a full development environment and a library of IP cores (GRLIB). Gaisler Research has a long experience in the management of ASIC development projects, and in the design of flight quality microelectronic devices. The company specializes in digital hardware design (ASIC/FPGA) for both commercial and aerospace applications. The products consist of user-customizable 32-bit SPARC V8 processor cores, peripheral IP-cores and associated software and development tools. The GRLIB architecture is mainly available through open source licensing, with commercial extensions.
Gaisler Research was acquired by Aeroflex Inc., in July 2008. Aeroflex is a global provider of high technology solutions to the aerospace, defence and broadband communications markets.

InformAsic AB				
Employees: 5	Personnel costs: SEK 3,593,840	Revenue: SEK 5,014,459	Operating Profit: SEK 215,555	Assets: SEK 1,741,165
Data from year 2007	Founded 2001			

InformAsic designs custom ICs for customers in the telecom and datacom industry. The InformAsic IP Cores for integrating Security and Cryptography in FPGA or ASIC designs have all been designed for flexibility, scalability, performance and ease of integration. The IP Cores are delivered with a project based license to be used in one FPGA or ASIC, and that can be instantiated one or several times in the same project design. InformAsic started in 2001 with the aim to offer its customers help in developing and delivering solutions built into cost effective integrated circuits with optimized functionality. The majority of the founders came from Ericsson, where they had been developing solutions at the front edge of technology and built personal networks within the international high tech industry. The customers are ranging from global high tech companies to SME with less competence and experience in designing electronic solutions. InformAsic takes the responsibility for the complete development process - from concept via prototypes to a finished product or component. They have also developed an ASIC for encryption of serial communication that has been delivered to security vendors. InformAsic is privately held and has its headquarters at the Chalmers Campus in Goteborg, Sweden.

Logipard AB.				
Employees: 10	Personnel costs: SEK 5,997,000	Revenue: SEK 13,117,000	Operating Profit: SEK 632,000	Assets: SEK 16,789,000
Data from year 2007	Founded 2006			
Logipard offers a portfolio of Video Codec IP Cores for implementation into customer ASICs and ASSPs. Our portfolio today consists of six generations enabling video codec functionality for all major codec standards such as H.263, H.264, MPEG-4, VC-1, AVS, MPEG-2 in resolutions up to full HD (1080p) The most important benefit of our solution is its very competitive Silicon footprint combined with its technical flexibility. Logipard is a spin-off from Anoto AB, which owns 80 percent of its shares. The rest is owned by the employees and management. In financial 2007, 77 percent of Logipard's costs were R&D costs.				
RealFast				
Employees: 4	Personnel costs: SEK 4,635,286	Revenue: SEK 4,372,367	Operating Profit: SEK -385,570	Assets: SEK 3,514,621
Data from year 2006	Founded 2001			
RFHC Realfast AB designs ICs for the automotive and industrial market sectors. The company has many years of experience in the areas VHDL/Verilog/FPGA/PLD/ASIC design and test/verification. The company also sells IP cores. The company is approved for HW/SW design of safety systems according to IEC 61508. RealFast had an innovation loan for 910.000 SEK, with conditional payback if a specific project would be commercialized or sold before 2010. The project was cancelled in 2006, and the loan was recorded as exceptional income for 2006.				
SP Devices (Signal Processing Devices Sweden AB)				
Employees: 15	Personnel costs: SEK 9,210,162	Revenue: SEK 4,993,360	Operating Profit: SEK -7,006,600	Assets: SEK 13,486,453
Data from year 2007	Founded 2004			
SP Devices' mission is to develop and market signal processing technology for enhancement of analog-to-digital (A/D) conversion. Our proprietary interleaving technology for digital post processing of parallel A/D-converters has been recognized for enabling ultra-high performance A/D conversion solutions. Our portfolio of products enable our customers to build systems with state-of-the-art A/D performance in the area of cellular base station transceiver (BTS) applications, digital imaging, high-speed data acquisition and broadband communication. At the beginning of 2007, SEB Venture Capital invested 30 million SEK in SP Devices. About 15 million SEK of new shares were emitted. In September, the firm took over Infineon's offices and equipment in Linköping, and hired Infineon's employees. At the end of the year the firm employed 20 persons.				
Wavebreaker AB				
Employees: 15	Personnel costs: SEK 11,160,000	Revenue: SEK 8,158,000	Operating Profit: SEK -7,170,000	Assets: SEK 2,409,000
Data from year 2006	Founded 2004			
Wavebreaker AB specializes in system-oriented Silicon-IP for wireless communications. The company has knowledge in the design of transceiver systems and integrated circuits for wireless data communication applications and is the owner of a broad technology portfolio. Wavebreaker designs IP and develops chip-sets for high data throughput transceivers with focus on multiple-channel RF transceivers and MIMO signal processing ASICs for WiFi. Wavebreaker's business mission is to be a strategic partner to IDMs and fabless IC companies in its area of expertise and to become a leading supplier of state-of-the-art Silicon-IP for complex wireless communications chip-set solutions. Wavebreaker was acquired by Flextronics International Sweden on 1 May 2005. Its operations were moved to Flextronics 1 May 2006.				

5.5 Where Did the IP Vendors Come From? The Innovation Model

An important question for policymakers is how new firms are born and what makes them grow. As was noted before, in the current networked economy, success factors are increasingly found from the dynamics of the business ecosystems and firm-specific factors do not explain successes and failures well. The innovation and growth models that underlie the development of IP firms and the whole industry segment would deserve further study. In this section, we briefly describe the emergence of ARM Holdings Ltd., as an example.

In general, the European IP industry consists of start-ups and spin-offs. Start-up firms are formed around an idea, and they build their organizations from scratch. There are at least three different types of IP start-ups in Europe. The first group consists of technology-oriented firms that are typically attempts to commercialize university research. Examples include Coresonic, a spin-off from Linköping University, and Recore, a spin-off from the Chameleon reconfigurable computing project at University of Twente. The second group consists of "business-oriented" firms, typically funded by venture capital firms that require aggressive growth plans. An example of this type of firm is Arteris, discussed above. The third start-up path is exemplified by the case of Bitboys, described in the previous section. This is essentially generated by technology enthusiasts who develop competences by addressing application-specific challenges.

A second, relatively large, set of firms consists of spin-offs from existing firms. These typically inherit organizational procedures, employees, and customers from the originating firm. European examples include ARC International, a spin-off from the Argonaut computer game firm, Silicon Hive, a spin-off from Philips, and the Swedish Logipard that was discussed in the previous section.

Policy can address many critical points along the development paths of high-tech firms. The different types of growth paths, however, require different policy approaches and tools. Often the most effective policy interventions are based on removing obstacles that unnecessarily increase business risks and slow down growth. In general, the tools have to be matched to the actual context where the firms evolve. These contexts are often complex and they consist of a mixture of factors that are not easily captured by any single disciplinary approach. To outline the contours of one well-known case, the next sub-section describes the development path of ARM, today the largest IP vendor, both in terms of revenues and employment.

5.5.1. The Case of ARM Holdings

ARM Holdings, plc. has it roots in the Acorn RISC Machine, developed in 1983-5 in the U.K.[85] The main designers were Roger (now Sophie) Wilson and Steve Furber. Wilson built the first Acorn microcomputer kit in 1978 while she was undergraduate at Cambridge University, based on her home-brewed designs. The ARM1 processor was designed to expand the success of Acorn's BBC Micro to business markets, and the processor architecture was inspired by the Berkeley RISC project.[86] As no commercial processors were available that could handle a graphical interface and the extensible BBC Micro architecture, Acorn's designers decided to build their own processor. The first commercial ARM product was the ARM Development System that allowed developers to write programs for the ARM processor using the BBC Micro. The second commercial product was ARM Archimedes, released in 1987.

85 For a compact review of the history of ARM, see Ferriani *et al.* (2007).

86 Berkeley RISC was developed by a group of students as part of their VLSI course between 1980 and 1984. Berkeley RISC, and the parallel Stanford MIPS reduced instruction set computing architecture projects became highly influential, the former leading, among others, to Sun's SPARC processors.

When Apple Computer was designing its new revolutionary Newton platform, it realized that only the ARM processor had specifications that were close to Newton's requirements. Newton needed low power consumption and it had to support static operation, where the processor clock could be switched off at any time. To develop the required extensions to the ARM architecture, Apple, Acorn, and VLSI Technology Incorporated, the manufacturer of ARM chips, jointly formed a new company Advanced RISC Machines, Ltd, in November 1990. The firm was later listed on the London Stock Exchange and changed its name to ARM Holdings plc.

Apple and VLSI both provided funding for Advanced RISC Machines, while Acorn supplied the technology. The 12 founding ARM engineers came from Acorn's Advanced Research and Development section that had developed the ARM processor.

With the introduction of its first embedded RISC processor in 1991, ARM signed VLSI as its initial licensee. One year later, Sharp and GEC Plessey entered into licensing agreements, with Texas Instruments and Cirrus Logic following the suit in 1993. After the 1993 addition of Nippon Investment and Finance (NIF) as a shareholder, the company began establishing a global presence, opening new offices in Asia, the US and Europe.

Although Apple's Newton gained some enthusiastic users, it never really succeeded in the market and the product line was cancelled in 1997. ARM, however, became highly successful as its processor cores were also particularly suitable for mobile phones that required low power consumption, small die area, and good performance at relatively modest processing speeds. Nokia, which did not have its own chip production capacity, became the key customer for ARM. In April 1998, the company listed on the London Stock Exchange and Nasdaq. More recently, in December 2004, ARM acquired Artisan Components, one of the leading US providers of low-level physical IP.

ARM cores are now used in about 90 percent of the world's mobile phones and ARM architectures have become almost de-facto standards for embedded general purpose processors in many domains. The main direct competitor is MIPS Technologies, based in Mountain View, California, which licenses a competing RISC IP core.

Of the nearly three billion ARM processor cores that shipped in 2007, almost two billion were shipped in mobile phones. In the same year, 42 percent of revenues came from customers in North America, 41 percent from Asia Pacific region, and 17 percent from Europe. Royalties from China-based chip designers increased by 27 percent, with seen new licenses signed with design teams in China during the year. ARM is now a global corporation with more than 1,700 employees and facilities in 12 countries on three continents, with design centres in: Blackburn, Cambridge and Sheffield in the UK; Sophia Antipolis in France; Bangalore in India; Sunnyvale, San Diego and Walnut Creek in California; Cary in North Carolina and Austin in Texas. The company also maintains sales, administrative and support offices in Belgium, China, France, Germany, Israel, Japan, Korea, Taiwan, Singapore, the UK and the US.

Industry experts agree that ARM is considerably ahead of Intel in designing processors for low power consumption and small silicon area.[87] This domain is critically important for mobile devices. Intel, therefore, is trying to improve its capabilities in this area, for example, using the Atom processor.[88] For a

87 See, e.g., Markoff (2008). Markoff characterizes ARM as an upstart, which obviously is not very accurate.

88 Historians of computing may note that the first Acorn computer was also called Atom. Acorn's Proton actually became renamed as BBC Micro. Both were designed by the same people who later designed the first ARM processors.

longer term, the real difference between the ARM designs and the Intel designs, however, may not be technical; whereas Intel is a traditional IDM with annual revenues of 40 billion USD, ARM is a pure IP vendor, at the core of a large network of synergistic and symbiotic business relations. Its own revenues are only half a billion USD; yet its economic impact is closer to Intel than normal business accounting would reveal.

A recent study by Ferriani *et al*. (2007) attempts to build a generic theoretical model of spin-off dynamics using the history of ARM as a starting point. As their study shows, successful firms never emerge from a vacuum, and often their success depends on events that can later be only described as lucky accident. In the case of ARM, the key success factor has been the vary rapid growth of mobile communications that occurred at the right time, putting the firm in the "sweet spot." From this location ARM was able to build a vibrant ecosystem and place itself at the centre of this ecosystem, establishing it as the global leader in general purpose pocessor IP.

6. Historical Drivers in the Intellectual Property Architectural Blocks Industry

The present business models in the semiconductor industry result from a long and idiosyncratic chain of historical events. Important historical factors in the development of the industry include military demand for reliable and small products, national industry policies, the emergence of new dominant technologies and end-product classes, and fast swings in business cycles.[89] More recently, the importance of demand from consumer electronics, fast product cycles, increasing costs of chip fabrication plants and design, and the availability of sophisticated design automation tools have become key factors in shaping the industry.[90]

The semiconductor industry is perhaps unique, however, in the extent incremental technical innovation has shaped its evolution. The continuous miniaturization of components on semiconductor chips –known as scaling–, steep learning curves, and the resulting rapid cost declines have led to fast expansion of semiconductor markets and new application areas for the technology. Due to fundamental physical factors, semiconductor industry has evolved in an economic context where product demand has been practically infinite.[91] The semiconductor industry is not a typical industry, and it is important to understand its rather unique dynamic also because it has considerable impact on the broader economy and society.

89 Cf. Morris (1990), Henderson (1989).

90 See, for example, Mowery and Rosenberg (1998), Langlois and Steinmueller (1999), and Brown and Linden (2009).

91 One should note, however, that the actual historical demand for semiconductors is not what economists usually understand with the concept. Semiconductor demand grows because new uses are found for ICs and the "demand space" expands. This demand space is in constant disequilibrium. Due to the large investment costs and granularity of investments in manufacturing capacity, the industry has also been very cyclical. For a discussion, see Tuomi, (2004b).

Below we describe some key drivers that have shaped the industry. These include the scaling and the resulting price declines, the increasing costs of manufacturing plant and IC design effort, and patterns of geographic expansion and concentration. The chapter also discusses the role of product standardization and variability as industry drivers, and highlights the possibility that historical trends will lead to the increased importance of product configurability in the future.

6.1 Semiconductor Scaling

Since the implementation of the first integrated circuit in 1958, with two transistors, the number of components on chip has grown tremendously. Currently the most advanced microprocessors contain more than 700 million transistors, and memory chips with 1.9 billion transistors have been demonstrated.

The continuing shrinking of feature dimensions on ICs and the resulting increase in component counts on semiconductor chips is known as Moore's Law. The law is named after Gordon Moore, co-founder of Intel, who in an influential article in 1965 discussed the factors that underlie the dynamics of scaling in integrated electronics. Common versions of the law state that the number of transistors on a chip, transistor density, cost per transistor, or the processing power of microprocessors, doubles approximately every eighteen months or two years. There exists very many variations on Moore's Law in professional and popular press.[92]

92 See Tuomi (2002b).

Intel now defines Moore's Law by stating that: "In 1965, Intel co-founder Gordon Moore predicted that the number of transistors on a chip would double about every two years."[93] IBM refers to the same article, claiming that Moore's Law says that component density is doubling every 12 to 18 months, and emphasizing that the Law only deals with the density of chips.[94] Both these statement are historically incorrect, as, in fact, Moore predicted that the number of transistors on the lowest cost chip would double annually, taking into account the component scaling, increase in the size of the chip, and advances in design practices.[95] In 1975, Moore reviewed his original estimate, and argued that the pace of development was slowing down, leading to a doubling of transistor counts in about two years. The two versions of Moore's estimates are shown in Figure 18, together with some historical data.[96]

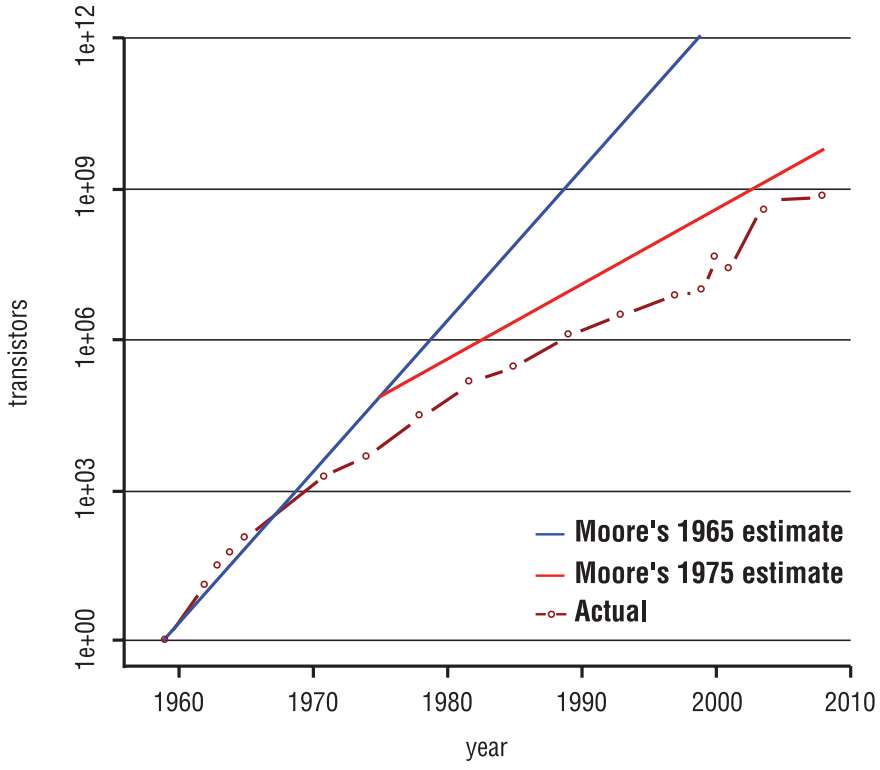
93 http://download.intel.com/pressroom/kits/IntelProcessorHistory.pdf. Intel, however, uses several incompatible definitions for Moore's Law. A backgrounder on Moore's Law claims that "Nearly 40 years ago, Intel co-founder Gordon Moore forecasted the rapid pace of technology innovation. His prediction, popularly known as 'Moore's Law,' states that transistor density on integrated circuits doubles about every two years."

94 E.g., Kahle (2006).

95 Moore (1965).

96 The historical data for the first decade include data that Moore used in his 1965 article for a graph on the number of components per integrated function. Moore's graph seems to represent the maximum number of components, and not the minimum cost chips that Moore discusses in his paper. Moore's graph starts at 1959, with one component. In 1959, two integrated chips existed: one by Kilby and one by Noyce. The former had two transistors and ten other components, and the latter had one transistor and six other components. We use the number of transistors in the graph above to make the numbers compatible with data from later decades. For post 1971 years, we use transistor counts of Intel microprocessors as given by Intel in a backgrounder on Moore's Law. This is actually somewhat misleading as only selected data points that fit relatively well with Intel's version Moore's Law are included. A data point for the Nehalem processor, introduced in November 2008 is included.

Figure 18: Moore's Laws



Source: Meaning Processing.

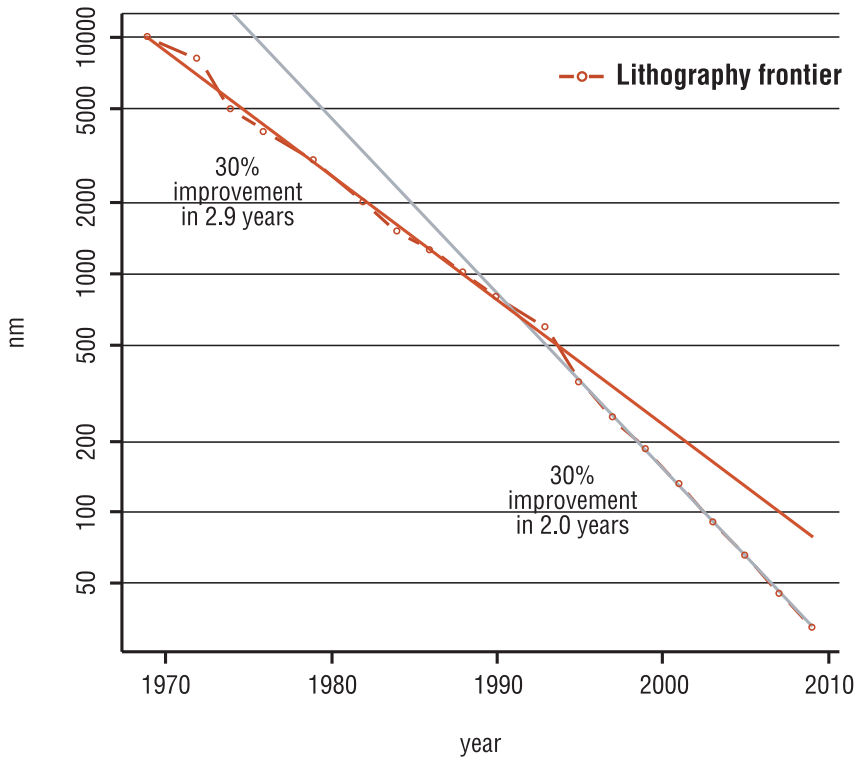
As even experts are confused about the definitions of Moore's Law, it is not surprising Moore's Law has become to resemble an urban legend. In fact, most variations of Moore's Law are both historically and empirically inaccurate.[97] An incontestable fact is, however, that miniaturization has been one of the main characteristics of and drivers in the industry. This can be seen from Figure 19 below, which shows the year of introduction of different generations of semiconductor wafer manufacturing processes. The first Intel microprocessor used a manufacturing process with 10 micron line width (10,000 nanometres). The last data point in the figure corresponds to the 32 nanometre process, which is expected to start in volume production in 2009.[98]

The figure also shows two lines that have been fitted to the historical data. As can be seen from the graph, developments in lithography have actually accelerated after 1994. When the linear dimensions of component features decrease 30 percent, the area used for the component decreases 50 percent, leading to potential doubling

97 In some cases, as for example with the authoritative International Technology Roadmap for Semiconductors (ITRS), we have been unable to find some of the historical chips that have been used to graph patterns of component counts. It seems that some fictive chips in the earlier decades are fitted to exponential growth curves as demanded by Moore's Law, instead of fitting the curve to historically existing chips.

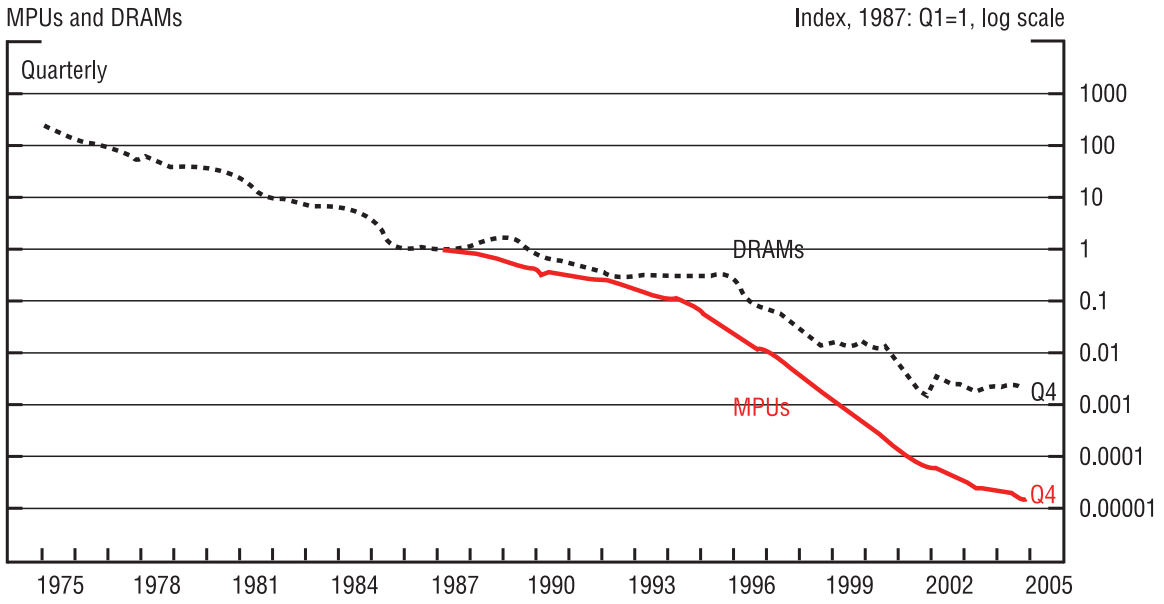
98 Technically, the line width is defined as "metal half-pitch," i.e., the smallest distance of two metal conductors on the chip. Other features may be considerably smaller. For example, insulator layers that are used to form transistors are now about 1 nm thick. Different features scale at different rates. For discussion and definitions, see: International Technology Roadmap for Semiconductors: 2007 Edition, p. 5. http://www.itrs.net/Links/2007ITRS/ExecSum2007.pdf. The data points refer to "lithography frontier," as reported by VLSI Research, except for the 45 nm and 32 nm processes, for which we use news releases. The 32 nm process uses double exposure and therefore is not, strictly speaking, comparable with the earlier lithography generations.

Figure 19: Year of introduction for process line widths



Source: Meaning Processing.

Figure 20: Constant-quality prices for microprocessors and DRAM memories



Aizcorbe et al.,2006

of the number of components.[99] In the 1970-1993 period, this improvement took about three years. Since 1994, it has taken about two years.

The continuing scaling of features in integrated circuits has meant that increasingly complex functionality has become possible on small chips. Shrinking physical dimensions also mean that electronic signals propagate faster. As a consequence, more information can be handled faster. Until recently, scaling implied better technical performance and also lower power consumption per calculation.

Enormous economic consequences have resulted from scaling, combined with the fact that the fabrication cost per semiconductor die area has remained almost constant for decades for leading-edge products. This means that the cost per transistor has declined at about the same rate as the component size. Smaller components on a chip have resulted in smaller costs. To put it the other way around, the same amount of money has bought every year radically more technical functionality. Year after year, this has opened completely new markets and applications for semiconductor technology.

The increasing performance of ICs and their declining costs have led to what we now know as the Information Society. It is, however, not easy to quantify the decline of cost. The speed of technical development means that comparisons across years cannot simply be made in normal inflation-adjusted currencies. A reasonable first approximation is, however, that the manufacturing cost per transistor of logic integrated circuits has declined 20 to 40 percent annually in the last decades. In the second half of the 1990s, heavy competition among manufacturers increased annual price declines in microprocessors to over 60 percent.[100] One of the most detailed

99 More accurately, the required linear scaling is , or 29.3 percent.

100 In the second half of the 1990s, also architectural innovations probably had an important role. For example, large amounts of on-chip memory were added to microprocessor chips. Transistors that are used for memory are much cheaper to design than logic circuitry, thus reducing the average cost per microprocessor transistor.

studies on the cost developments concludes that the constant-quality microprocessor prices per transistor declined at an average annual rate of 30 percent during 1988-1994, reaching an extraordinary rate of 63 percent in the 1994-2001 period, slowing down to 40 percent in 2001-2004 period.[101]

6.1.1. The End of Scaling

Scaling, however, has also led to important challenges. These include theoretical and practical problems in extending photo-lithographic manufacturing methods to feature sizes that are smaller than the wavelengths of ultraviolet light used to expose chip layers.[102] Moreover, as the component sizes in advanced semiconductors approach atomic sizes, traditional semiconductor technology will eventually hit basic physical limits. The isolation layers in a leading-edge ICs are now about 1.1 nanometres thick, corresponding to less than five molecular layers. Industry experts usually agree that there are no existing viable lithography solutions beyond the 32 nm process, to be in production before the end of 2009. The basic technologies for the next 22 nm process generation are being developed in laboratories but either it or the following 16 nm process is already expected by many experts to be the final limit for the traditional planar technologies.[103] If the process nodes would follow each other every two years, lithography scaling would therefore end in about five years from now.

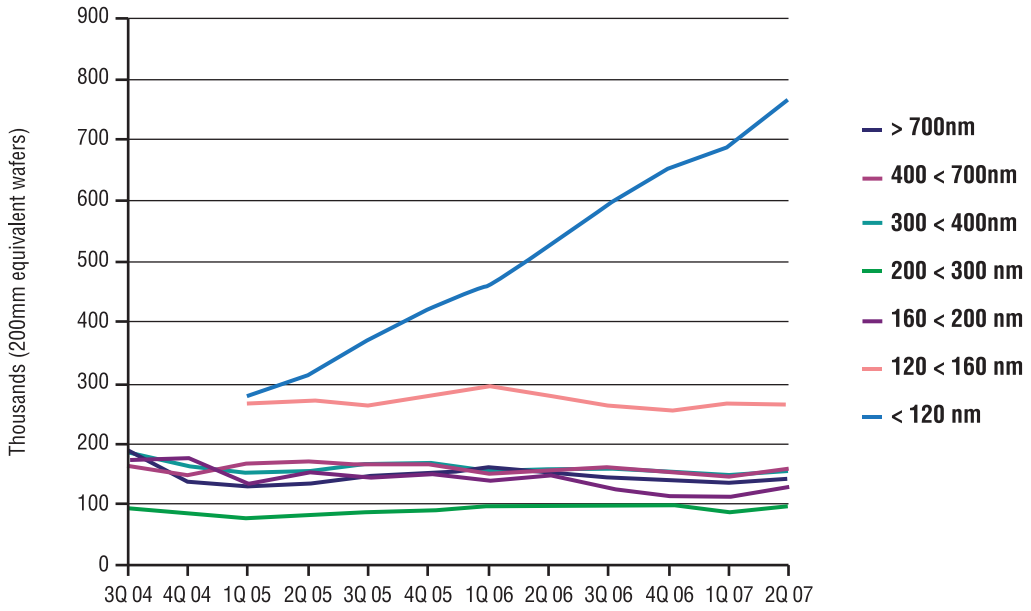
The fundamental physical limits of scaling have already changed semiconductor design and manufacturing processes.[104] Although new process technologies allow an increasing number of transistors to be placed on a chip, many of these transistors are now used to overcome problems created by scaling. For example, advanced microprocessors use an increasing number of transistors to switch off parts of the chip so that the chip does not melt down. In complex semiconductors, the effective number of transistors grows much slower than their total number. For example, modern double core microprocessors power down one of the processors on the chip when power consumption becomes more important than processing power. Similarly, designers manage harmful component variance by replacing single transistors with several parallel transistors, as well use dummy transistors to stabilize the electrical characteristics of transistors that are actually used on the chip.

6.1.2. The Long Tail of Semiconductor Products

As bleeding-edge technologies often gain visibility in the media, it is important to note that older technologies are also widely used. This can be seen in Figure 21, which shows recent global data for actual wafer starts, based on Semiconductor International Capacity Statistics (SICAS). For example, whereas Intel moved to 250 nm technology in 1997 in its microprocessors, in the second half of 2007 about 27 percent of wafer starts were still for chips with over 300 nm half-pitch. In the first half of 2008, almost a fifth of semiconductor wafers were still using these technologies that were behind the leading edge over ten years ago. Although the most advanced technologies grow rapidly after their introduction, as they are used for the highest-volume chips, the old technologies do not fade away. The rapid growth of leading-edge, visible in Figure 21 as the "less than 120 nm" category, also partially results from the fact that the data do not differentiate the most advanced technologies, which become aggregated in the category as new technology generations are introduced.

101 Aizcorbe, Oliner & Sichel (2006).
102 Cf. Yoshioka (2005).
103 In his Common Platform Technology Forum presentation, 30 September 2008, Gary Patton, vice president for IBM's Semiconductor Research and Development Center, stated that lithography will hit a discontinuity at 22 nm.
104 Cf. Solomon (2002). In the 32 nm process, traditional exposure is being replaced by "computational scaling," where the desired features are formed by multiple exposures of ultraviolet light through masks that contain patterns that are calculated using computers. The mask layouts, therefore, do not resemble the physical structures of the chip.

Figure 21: Actual wafer starts in different technologies, 3Q 2004 - 2Q 2007



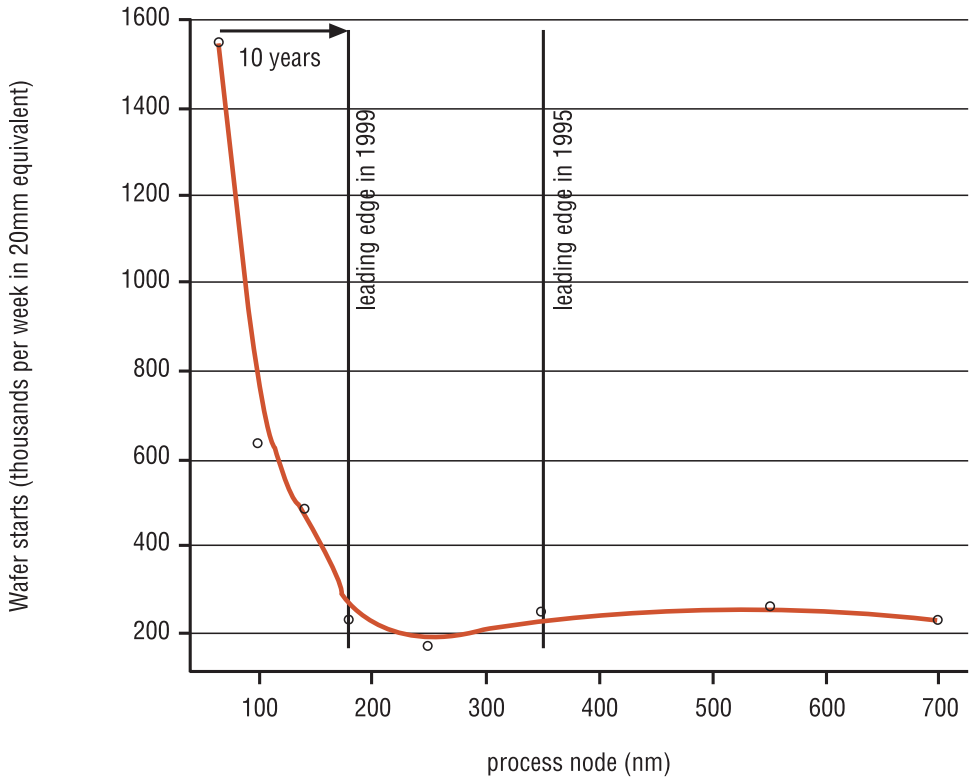
Source: SICAS, 2007.

The number of semiconductor wafers created in the first half of 2008 in different process technologies is shown in Figure 22, based in SICAS data. The data do not separate wafers manufactured in the two most advanced technology generations in use today (65 and 45 nm), and these are both included in the "less than 80 nm" category. In fact, leading-edge lithography moved below the 80 nm generation in 2004. The relatively high volume of wafers in the most advanced process category, therefore, reflects the total volume in all technology generations introduced since 2003. SICAS data are also based on reports from the participating companies, which tend to be the biggest leading-edge firms, and it therefore undercounts production in older technologies. Also because the leading-edge technology is mainly used for very high-volume products, including PC microprocessors and memory chips, the share of these advanced wafers is relatively high. One should, however, note that except a small number of high-volume products, the vast majority of products is manufactured in technologies that are several generations older than the current state-of-the-art. For example, the leading European foundry X-FAB, which does not participate in SICAS, focuses on analog and mixed-signal chips and offers foundry services in the 180 nm – 1000 nm range.

It is impossible to understand the evolution of semiconductor industry without the impact and effects of scaling. At the same time, it is impossible to understand the future of semiconductor industry without considering the effects of the end of scaling. Although there are many uncertainties, it is clear that the industry will take seriously the possibility that this key driver for the industry will disappear in about ten years time. Given that the investment required for leading-edge semiconductor manufacturing plant is now counted in billions of US dollars, it is clear that the investors will carefully consider whether they are approaching a technology dead-end in the next decade or so. New business models will emerge, and it is increasingly probable that currently dominant value chains will be reorganized in the next years. As the semiconductor industry has been the most important driver for macroeconomic productivity growth since the early 1990's,[105] this

105 Tuomi (2004b).

Figure 22: The long tail of semiconductor technology, 2008



Source: Meaning Processing.

restructuring will have profound impact on the broader economy and society.

The International Technology Roadmap for Semiconductors (ITRS) now extends to year 2020. It is currently debated whether CMOS technologies, or any other semiconductor technologies, can actually keep on scaling until that time. Although radically new nanotechnologies and maskless electron beam technologies could in theory continue the miniaturization of digital technologies, in the near future they can not be used for producing economically viable components.[106] A recent industry estimate puts the availability of nanotechnologies as replacement for CMOS to beyond 2030.[107] In his recent interview, Moore noted that he believes that the scaling can continue perhaps 10 or 15 years, but that "no exponential can grow forever."[108] More importantly, it is unclear at present whether it is economically feasible to continue scaling up to its technical limits.

6.2. Manufacturing and Design Costs

The evolution of business models in the semiconductor industry has been greatly influenced by the fact that IC fabrication costs have been rising fast and very large investments are now needed when new leading edge manufacturing plants are set up. In 2007, a new leading-edge fabrication

106 Recent advances in maskless direct-write e-beam lithography could make it a viable alternative for some low volume products when combined with appropriate design methods, see (Fujimura 2008).

107 Pele (2008a).
108 Moore (2007).

plant required a USD 3.5 billion investment.[109] Typically fab costs are also partly covered by public funding and investment incentives. Fab costs are projected to be in the USD 5 – 10 billion range in the 32 nm process to be in production in the second half of 2009.[110] IC Insights estimates that if a company manufactures its own products at 32 nm, it must generate more than USD 16 billion in annual revenue to achieve an acceptable return on investment. Only two firms, Intel and Samsung, have revenues in this range.

The increasing costs of semiconductor wafer fabs is commonly known as Rock's Law, or "Moore's Second Law." It states that fab construction costs double about every four years. The law is named after Arthur Rock, one of the first venture capitalists, who helped to set up Fairchild Semiconductor and several of its spin-offs that later established the Silicon Valley.

In 1965, the cost of setting up a state-of-the-art semiconductor manufacturing plant was USD 1 million; by 1980 the cost had escalated to about 50 million.[111] In 1985 a semiconductor fab cost about USD 100 million, when the industry generated total revenues of about 22 billion.[112] In 2007, when the industry had record revenues, the cost of state-of-the-art 45 nm plant was 1.5 percent of the total industry revenue. This may be compared with the average fab cost that in 1960 was about 0.125 percent of the total industry revenue. For the leading-edge 32 nm technology, the cost will be 4 percent or more of the total industry revenues in 2009, depending on the impact of the current economic downturn. In addition, the R&D investment in process development for leading-edge 32 nm technology is expected to be about USD 3 billion.[113]

Rock's Law is empirically inaccurate, partly because the leading firms have learned to slow down the growth of costs. It illustrates, however, the point that fabrication facilities are now beyond the reach of almost all potential investors. Strictly speaking, there are only two or three companies, Intel, Samsung, and maybe Toshiba or TSMC, and perhaps one country, China, that can make the required investment.[114] This is the main reason why, with the exception of Intel, the firms are now clustering around industry alliances that share the costs for research in future process technologies.

As the designs become more complex, also design costs rapidly increase. A chip with millions of transistors cannot be designed without automated tools. The revenues for the three leading electronic design automation (EDA) tool vendors, Cadence, Synopsys and Mentor Graphics were USD 3.7 billion in 2007. It has been estimated that the annual software expense for a small semiconductor company was about USD 10 million in 2002, and that a company that earns below USD 1 billion would be below the efficient scale for in-house design.[115] The license fee for a state-of-the-art EDA tool can now be several hundred thousand dollars per designer seat.

The design of complex ICs consists of both defining and testing the hardware and the software that makes the hardware useful. Brown and Linden (2009) quote data that shows that about half of the total hours needed to engineer a chip in the 130 nm digital logic process is used for software development. In the 90 nm process, software was responsible for about 45 percent of the total design investment, rising to 65 percent in the 45 nm process.

109 Intel's newest USD 3.5 billion fab in Kiryat Gat, Israel, was inaugurated in July 2008. Intel is also investing USD 2.5 billion in a new wafer fabrication facility in Dalian, China. The Dalian Fab 68 is Intel's first new wafer fab at a new site in 15 years. Due to export restrictions the fab will probably trail two or more technology generations the leading edge when it starts operations in 2010.

110 GSA puts the cost of a 300 mm 32 nm fab at USD 10 billion. This probably includes process R&D costs.

111 Saxenian (1981).

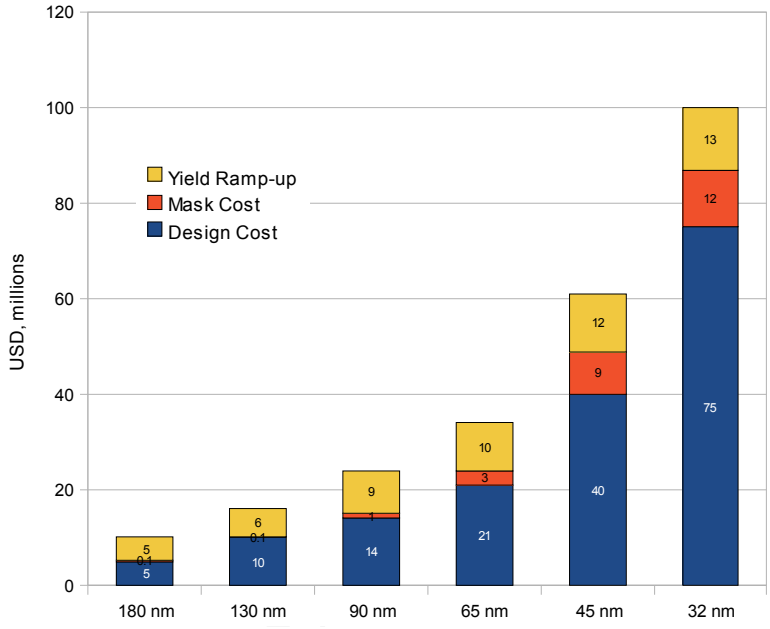
112 Kanellos (2003).

113 Ng (2008).

114 As noted below, ATIC, based in Abu Dhabi, has also recently invested in fabrication capacity.

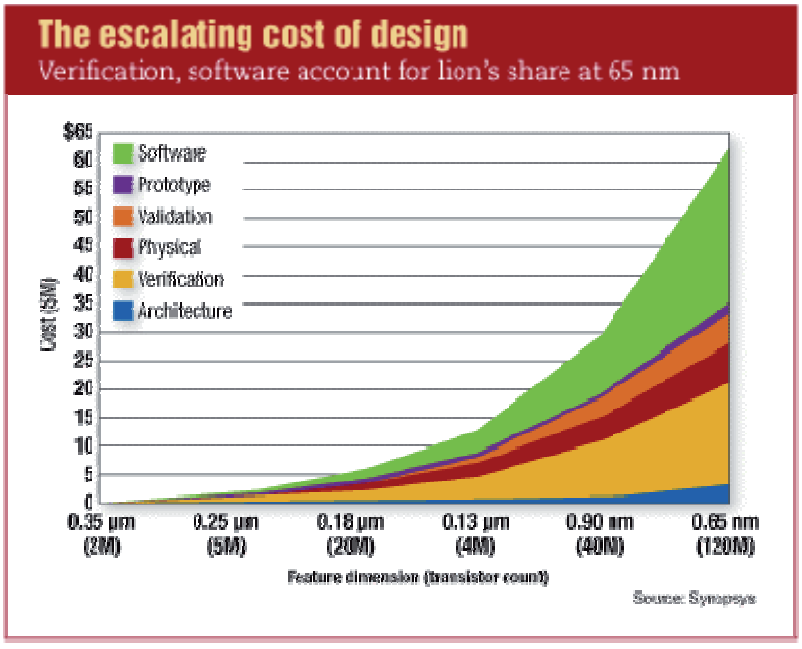
115 Brown and Linden (2009).

Figure 23: IC design costs at different process nodes



Source: Data from Chartered, Synopsys, GSA

Figure 24: Design cost breakdown



Source: Synopsys.

The overall costs of producing digital chips is shown in Figure 23, based on data from Chartered, Synopsys and GSA.

As the complexity of designs increases, it also become increasingly difficult to test the fabricated chips. In addition to software costs, verification costs have been escalating rapidly as new technology generations have been introduced. This can be seen from Figure 24.

6.3. Local Ecosystems and the Asian Competition

Semiconductor industry has been among the leaders in globalization since the early 1960s. As Jeffrey Henderson (1989) has shown, in its early phases, the industry generated a social and technical division of labour that is quite unlike those of most industries. Semiconductor production has since the 1960s been characterized by its vertically disaggregated or "technically disarticulated" labour processes. In other words, production in the industry consists of relatively independent clusters of work tasks, such as design, chip fabrication, assembly, packaging and testing that require different labour processes. As a result of this disarticulation, production processes in the semiconductor industry have been globally distributed to an extent rarely seen in other industries.

Technical developments and the rapid growth of market size have also provided opportunities for the emergence of specialized firms that fulfil dedicated roles in the production system. The semiconductor industry, therefore, is the prototypical example of a business ecosystem that has developed through a large number of spin-offs. In the first decade of integrated circuit history, in the 1960s, internationalization of production occurred mainly inside multinational corporations, and spin-offs from these MNCs generated geographically concentrated local hubs. Since the late 1980s, the global distribution of production has, however, essentially followed the network model, creating a fundamentally global system of production. In this process, different geographic regions have emerged as globally connected specialized hubs.

During its history, the semiconductor industry has also created the most prominent local concentration of high-tech production, the Silicon Valley, in Santa Clara County, California. Numerous analysts have studied the emergence and development of Silicon Valley, and many policymakers have tried to imitate its success in other regions of the world.[116] In most cases, these imitations have proven to be unsuccessful. Partly this is because some of Silicon Valleys key success factors, indeed, are historical factors that are difficult to replicate in other times and other regions of the world.

The basic dynamic of simultaneous globalization and regional concentration of semiconductor activities drives also future developments in the industry. As the present study also tries to analyze the extent to which semiconductor IP and design activities could relocate to Asia and China, it is useful to recall the key drivers in this dynamic.

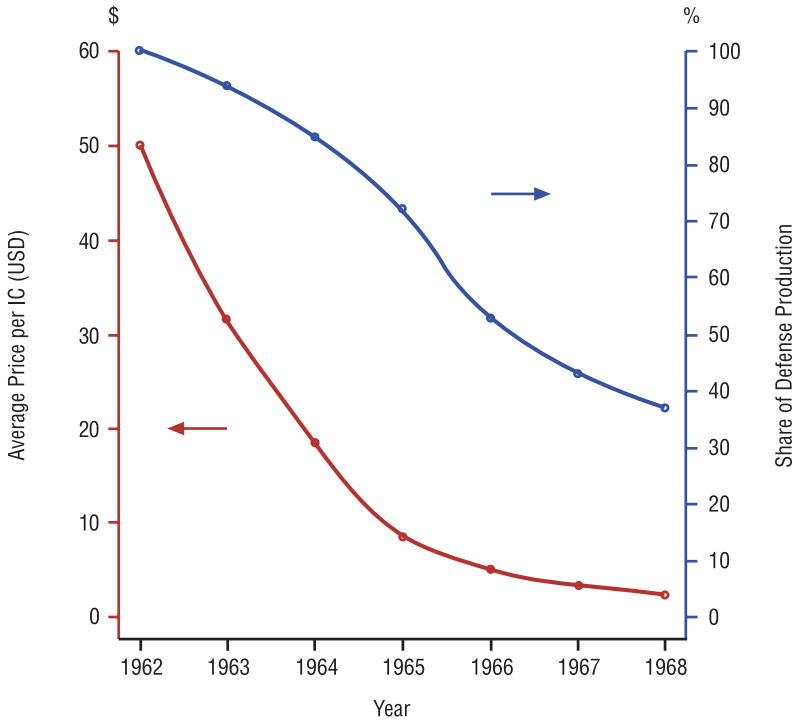
6.3.1. The Local Global Hub: Silicon Valley

In the 1950s, several factors facilitated the move of the nascent semiconductor industry from the Northeast US to Santa Clara. These factors included the increasing influence of labour union organizations in Northeast, the anti-trust law suits that forced AT&T to liberally license semiconductor technology, the growth of post-War defence industry in California, as well as the proximity of the large teaching and research centres in Stanford and Berkeley. The origins of the Silicon Valley can be traced back to the 1950s; the name, however, first appeared in the 1970s, about a decade after Fairchild Semiconductors had set up its first offshore operation in Hong Kong. The "secret" of Silicon Valley, therefore, cannot be found simply by searching it from Silicon Valley; instead, it is to be found from the new global distribution of labour and production that has allowed Silicon Valley to become a central coordinating node in the semiconductor industry.

The historical concentration of semiconductor-related activities in Silicon Valley partly results from the very rapid growth of the industry, which expanded at about 15 percent per year in real terms

116 See, for example, Castells and Hall (1994) and Kenney (2000).

Figure 25: Share of military production and average price of ICs in the US 1962-1968



Source: Meaning Processing.

in the 1960s. Inside Silicon Valley, this lead to a rapid increase in the number of semiconductor firms, often through spin-offs. Fairchild Semiconductor, alone, generated about fifty companies between 1959 and 1979. The rapidly growing market for semiconductors also generated new opportunities for vertical disintegration and specialized labour. As a result a rich ecosystem emerged, where many different types of firms provided expertise, first in manufacturing equipment, and later in silicon wafer production, optical mask production, test and measuring instruments, and in other parts of the value chain. In the early phases of vertical disintegration, geographical proximity was an important factor, as the technologies in use were extremely unstable and the complex system of specialized actors greatly benefited from regular face-to-face contacts. Silicon Valley was also a low-cost region. In the late 1970s, the wage rates in Silicon Valley were about 30 to 60 percent lower than in Northeast, partly because of almost non-existent labour unions in Silicon Valley. The majority of the industry's low and semiskilled production workers were immigrant Latino and Filipino females, who resided in the San Jose area (Henderson 1989).

The growth of the Silicon Valley ecosystem occurred partly through a formation of many specialized producers that addressed demand in different product niches. The product volumes were low and the production system, therefore, was based on small batch production. Partly the reason was military demand, which represented about 50 percent of all semiconductor production in the 1960 in the US. In the first years of the 1960s, military demand was critical for the IC industry and the formation of the Silicon Valley, allowing US firms to recover research and development costs for new products. This can be seen in Figure 25, which shows the share of military production of total IC production in the US, as well as the average price of ICs sold in 1962-68.[117]

117 Data from Tilton (1971, 91). Mowery and Rosenberg (1998, 133) use the same data, quoting only the original data sources.

Towards the mid-1960s, however, semiconductors were increasingly used for consumer electronics, leading to larger product volumes. The increasing demand from consumer electronics also created increasing opportunities to internationalize semiconductor production, as the earlier demand from military uses also meant that only domestic US manufacturers were allowed to produce the components.[118] The US firms easily maintained their competitiveness in advanced high-performance components as the demand in Europe was mainly in industrial applications, and in Japan the demand focused on cost-sensitive consumer electronics. In contrast to Europe, where governments typically gave military contracts to defence-oriented firms, the US practice was to order defence-related products from industrial and business equipment firms, who often were allowed to use new and untried technologies.[119] As a result, new semiconductor innovations were typically introduced in Europe and Japan about two years behind the US in the 1950s and 1960s.[120]

One factor that has enabled Silicon Valley to become a focal point in semiconductor technologies is the fact that it, quite literally, was a green field operation, built on orchards and citrus fields. The institutional infrastructures of the region have co-evolved with the industry, leading to a very efficient industrial system. The need to manage spin-offs has created services and knowledge that supports small rapidly growing technology firms. This is in contrast with many European locations, where existing industrial and institutional structures have provided the context for the growth of the semiconductor industry.

Silicon Valley and its infrastructures were also born at a time when face to face contact was important for knowledge transfer and creation. Semiconductor spin-offs were built on a complex social network, where key persons were connected through tight social networks.[121] Knowledge, therefore, was effectively shared and accumulated social capital increased the efficiency of business transactions.

Also intellectual property rights had a great impact on the development of the IC industry in Silicon Valley. AT&T, and its research arm, Bell Laboratories, licensed freely the core transistor patents and shared the related knowledge, partly as a result of an antitrust suit initiated by the US Justice Department in 1949. A consent degree ended the antitrust proceedings in 1956, requiring AT&T's manufacturing arm, Western Electric, to license any of its existing patents royalty-free to any US firm and all future patents at reasonable royalties. As Tilton points out:

> "Certainly the great probability that other firms were going to use the new technology with or without licenses is another reason for the liberal licensing policy. Secrecy is difficult to maintain in the semiconductor field because of the great mobility of scientists and engineers and their desire to publish. Moreover, semiconductor firms, particularly the new, small ones, have demonstrated over and over again their disposition to infringe on patents. The prospect of lengthy and costly litigation in which its patents might be overturned could not have been very attractive to AT&T. Even if successful, such courtroom battles pitting the giant firm against small rivals damage public relations.[122]"

AT&T had most of the key patents for semiconductors, and it extensively cross-licensed these patents with other industry actors. In practice, industry actors had to join the AT&T bandwagon, and patents and related knowledge were widely shared. As Gordon Moore once noted:

118 Henderson (1989, 44).
119 See Mowery and Rosenberg (1998, chap. 6).
120 Tilton (1971).
121 See Castilla *et al.* (2000).
122 Tilton (1971, 76).

"Well, it was probably a different attitude about patents. One thing that happened in the semiconductor industry... semiconductor processes are a long series of steps and the patents had gotten pretty broadly spread because all of the people working on the technology had some of them. And the net result was in order for any of us to operate we had to be cross-licensed so the participants tended to all cross-license one another. So, there was not a tremendous advantage to having more patents... with a couple of exceptions, there wasn't much net benefit from it.[123]"

Patenting policies in the semiconductor industry changed in the 1980s.[124] One may, however, argue that the foundations of Silicon Valley, as an innovative R&D intensive region, were already fully in place at this time, and that the current strong patent protection policies have not been important for the ICT industry growth in Silicon Valley.[125] As a result of the strengthening of the IPR regime in semiconductors in the 1990s, patent portfolios became increasingly important for cross-licensing. The dynamic impact of strong patent protection was perhaps mainly visible in the slowing down competitors in an industry where system compatibility and first-mover advantages are critical.

The rise of Silicon Valley is, therefore, bound to a specific phase of the development of the IC industry, where early military demand and the rapid growth of markets allowed new firms to create new technologies, and where competent engineers rotated among the firms, enabling rapid competence development and broad sharing of critical knowledge. At the same time, the institutional infrastructures of Silicon Valley, ranging from venture capital and law firms to university education and service providers, became specialized in serving the rapidly growing business. Similar processes of mutual institutional adjustment and historically developed social networks are, obviously, difficult to create today. Some policy initiatives, however, aim at "ecosystem" development in ICTs. These initiatives move beyond the conventional industry cluster policies by taking into account a broader set of actors, including the users.[126] For example, South Korea is now implementing a policy initiative that tries to develop its SoC ecosystem, including semiconductor design. As successful open source software projects have shown, today it is also possible to create geographically distributed development hubs where knowledge flows effectively beyond regional boundaries. The future global innovation hubs, therefore, only remotely resemble the historical model of Silicon Valley, which, itself, now to a large extent operates on the Internet.

6.3.2. The Move to Asia

American firms totally dominated the world semiconductor production until the early 1980s, although much of their production actually occurred outside the US. The internationalization of the US firms was first driven by two factors: the increasing competition in discrete semiconductors from Japanese semiconductor firms, and the increasing product volumes that enabled disaggregation of the production process. First, this process led to the establishment of semiconductor activities in East Asia, contributing both to the economic development of the four Asian Tigers

123 Moore (1995).
124 Hall & Ziedonis (2001).
125 In fact, the current strong patent protection policy in the semiconductor industry was initiated by Texas Instruments, perhaps because it had to compensate its competitive disadvantage in accessing the Silicon Valley innovation system. Software patents, of course, were important in the last years of the 1990s. Their importance, however, probably was to a large extent symbolic, as they were viewed as a condition for getting venture capital. In a sense, software patents were used as poison pills that made it expensive for competitors to slow down firm growth by binding managerial and financial resources in lawsuits.
126 Examples include some of the European Living Labs and some national initiatives, such as the Finnish ICT SHOK (one of the Finnish Strategic Centres for Science, Technology and Innovation). In general, although the term ecosystem is now widely used, there are no well-developed research-based frameworks for ecosystem policies.

or Dragons, also known as the "gang of four": Hong Kong, South Korea, Taiwan, and Singapore, and to policy discussions on the potential decline of earlier high-tech superpowers. Second, in the 1990s, the liberalization of investment and trade policies in India created a rapid surge of offshoring and outsourcing of ICT-enabled services, including software programming and semiconductor design to India.

6.3.2.1. East Asia and the Four Dragons

The most important determinant in the growth of semiconductor production in East Asia in the 1960s and 1970s was the presence of enormous pools of cheap and underemployed labour. Cheap labour, however, was not the sole factor at play. The US firms first entered East Asia through Hong Kong, which had several special advantages that made it a particularly attractive location. According to Henderson, these included political stability, an open financial system with no limits on repatriation of profits, and excellent telecommunications and transport facilities. These characteristics were shared by Taiwan, South Korea and Singapore. Hong Kong, however, had also the added advantage that in the 1950s it had developed a flourishing industrial economy based on textiles, garments, plastics, and other labour-intensive forms of production. It had, therefore, well developed international trading networks and logistic capabilities. By the late 1950s, Hong Kong had extended these production models to electronics products, becoming a major location for radio assembly.[127]

Fairchild Semiconductor established the first semiconductor assembly plant in Hong Kong in 1961. General Instruments followed the suit, setting up the first semiconductor plant in Taiwan in 1965, and Fairchild and Motorola then moved to South Korea in 1966. By 1968, Texas Instruments, National Semiconductor and Fairchild had set up plants in Singapore. Malaysia followed in 1971, and Philippines , Thailand and Indonesia a couple of years later. As Henderson notes, by the mid-1970s, US semiconductor plants had been established in every capitalist East Asian developing society other than Brunei.

Development, however, was not evenly distributed. Most of the production in East Asia was by US firms for the US markets. Control of production, as well as the most knowledge-intensive tasks, were strongly concentrated in the US. Only the most labour-intensive assembly processes were done in East Asia, with the exception of those territorial units, Hong Kong and Singapore, which gradually gained marketing responsibilities. All the firms assembling semiconductors in the region used basically the same model: the wafers were fabricated in the US, air-freighted to East Asia, assembled into discrete semiconductors or integrated circuits, and then air-freighted back to the US for final testing. This arrangement was partially encouraged by the US tariff regulations that charged import duty only on the value added abroad. As the offshore value added was mainly generated by cheap unskilled labour, import duties remained a relatively low barrier for such international division of labour.[128]

By the mid-1980s, the international division of labour in the semiconductor industry, however, had started to change. In particular, Hong Kong, Singapore, Taiwan, South Korea, and to a lesser degree Malaysia, had started to climb the value ladder, whereas Thailand and Philippines were increasingly focusing on large-batch production that relied on low-cost labour. Hong Kong and Singapore were increasingly moving from assembly to more demanding parts of the value chain, including testing and, to some limited extent, design. Partly the emerging division of labour within East Asia resulted from the fact that Hong Kong, Singapore, Taiwan and South Korea all had educational systems that could produce skilled workers. Partly it resulted from the fact that the labour costs started to increase rapidly in these countries. In some cases, as in Singapore, wage

127 Henderson (1989, 51).

128 Henderson (1989, 54).

increases were driven by explicit policy, aimed at pushing the country towards higher-value adding production. The end result was, however, a new regional architecture of production, where an increasing number of tasks were done within East Asia, and where partially finished goods moved from one East Asian country to another, until the final products were shipped to the developed economies of the world.

Until the mid-1980s, and with the exception of some Japanese and European firms, this East Asian international division of labour was tightly controlled by US firms and most plants were set up by foreign investment. Towards the end of 1980s, the situation started to change. In 1985, Hong Kong had four locally owned wafer fabrication and assembly plants, whereas South Korea had five and Taiwan eight.[129]

Policy was a critical factor in establishing this indigenous production capability. In all the four "Asian Tigers," electronics and semiconductors were perceived to be critical technologies for development. For example, the Korean government provided a continuous flow of low interest capital to semiconductor firms and it has also invested heavily in semiconductor R&D. The heavy involvement of the government also allowed the Korean policymakers to systematically plan for the development of the industry. An important factor in the growth of the indigenous semiconductor industry was also protectionist trade barriers that included formal import duties and also informal barriers. Korea, for example, imposed a total import ban on foreign-made electronics in the early 1980s, which was lifted only in mid-1990s. This meant that foreign producers could access the rapidly growing Korean market only by producing inside Korea either through fully-owned subsidiaries or joint-ventures, or by licensing their technology to Korean producers. Similar trade barriers were applied in Taiwan, where, for example, the imports of Japanese VCRs were forbidden in the early 1980s, and where import duties in other electronics products during the 1980s were often close to 50 percent.[130]

Relying on technology licenses from US, Japanese and European companies, Korea gained a substantial part of the world market on memory chips towards the end of 1980s. Originally, the Korean semiconductor industry was built around semiconductor divisions of the four chaebols, Samsung, GoldStar, Hyndai and Daewoo. Samsung and Hynix, formerly Hyndai Electronics, started to produce dynamic random-access memory (DRAM) chips in 1983. Today, Samsung is the second largest and Hynix the eight largest semiconductor producer, worldwide.

Korea has now some 260 design houses with total revenue of USD 1.5 billion.[131] About ten percent of the design firms are in ASIC services. The Korean IT SoC Association (ITSA) estimates that Korea has 100 firms that specialize in System-on-Chip development. This area has also been one of the focal areas in the Korean Information Society Strategy. The Korean government believes that System-on-Chip represents the next step in climbing the value ladder, and that the SoC industry will be a major source of exports and employment in the next years. The Korean policymakers, therefore, are establishing a national ecosystem that supports the SoC industry, organized around ITSA. The government also aims at the standardization of the semiconductor IP production processes and process interfaces, hoping to speed up SoC production. The government also vitalizes the Shuttle Run system for multi-project wafers. The investments in the SoC industry are expected to enable Korea to gain ten percent of the global SoC market by 2010 and create 50,000 jobs in related fields.

Singapore, in turn, has now about 40 IC design houses and 14 silicon wafer fabs, and 20

129 Scott (1987).

130 Aw *et al.* (2001).

131 ECN Asia (2008).

assembly and test companies. EDB estimates the total number of IC design engineers in Singapore at 1,250 in 2007, and projects it to grow to 1,760 by 2009. As Singapore is starting to lose manufacturing operations to low-cost regions, including China, Malaysia and Vietnam, the government has adopted a three-pronged strategy to strengthen Singapore's semiconductor industry. First, it will support the growth of the wafer fabs to better economies of scale. Second, it will support process R&D that will ensure that the wafer fabrication plants are able to stay at the leading edge. Third, it aims at developing a vibrating semiconductor ecosystem. The objective is to provide a complete end-to-end system where IC design houses, IP providers, foundries, system design firms and EDA companies are integrated under the auspices of Microelectronics IC Design and System Association (MIDAS).

According to Industrial Technology Research Institute (ITRI), Taiwan's IC design sector will reach USD 14.25 billion in 2008. ITRI estimates that there were 350 design houses in Taiwan, of which 272 were local operations, in 2007.

In general, the key factor in the rapid growth of economies in Japan and the Asian Tigers is a simple one. East Asia become a powerhouse of electronics and semiconductor industries because of massive policy interventions. As Henderson points out:

> "When one recognizes that these states (including Hong Kong) are precisely those that in the dream world of *laissez-faire* theorists are economic 'success stories' because of their supposed commitment to non-intervention, then one begins to get some measure of how ideological (not to mention empirically wrong) the dominant neo-classical paradigm in economics is. In spite of the fact that we are dealing with formally different states –repressive military dictatorships in South Korea (at least until 1987) and Taiwan, and authoritarian democracy in Singapore, and an autocratic colonial regime in Hong Kong – in all cases, economic development in these societies must now be seen, if anything, to be state-led."[132]

Not unsurprisingly, then, that semiconductor production has been one of the main themes in policy debates also outside East Asian countries. In the 1980s, it was one of the most heated topics in the US – Japan trade relations. From late 1970s on, Japan rapidly gained dominance in the DRAM memory industry, when Fujitsu and Hitachi advanced beyond Intel as the leaders in DRAM production. Japan also started to create globally visible ambitious nationally coordinated projects in electronics and computing. These included the Fifth-Generation Computer Systems project that was to implement massively parallel computing architectures with artificial intelligence user interfaces.[133] As a response, the US government threatened to set punitive import duties on Japanese semiconductors, and set up their own Microelectronics and Computer Technology Corporation (MCC). Also the U.K. Alvey project and the EU ESPRIT aimed at responding to the emerging Japanese challenge. Among the US policy makers, the Japanese challenge was described as the "new Pearl Harbor."

The growth of the Asian Tigers has created less controversy, probably because of three reasons. First, the East Asian export-oriented policies were generally aimed at attracting foreign investments from established semiconductor firms, based in the US, Japan and Europe. The policies, therefore, were often beneficial to the established firms. Second, both the semiconductor and the broader electronics industry were already globalizing in the late 1980s. Centrally controlled international firms were being transformed into multinational and multi-domestic enterprises that were managed as complex matrices of relatively independent profit centres. This development became possible when the rapidly declining communications

132 Henderson (1989, 72).
133 For a US perspective, see Feigenbaum and McCorduck (1983).

costs allowed increasingly tight integration of knowledge-intensive tasks across geographic distances. Industrial interests, therefore, were not, anymore, easily drawn along country borders. As Robert Reich (1993) put it, it was not clear "who is US." A third factor that muted some militant voices declaring an imminent doom of the US technology leadership was the simple fact that the rapid growth of personal computing strongly favoured US semiconductor makers. This was partly because when Intel started to lose its fight against Japanese memory makers, it dropped the memory business and focused on CMOS microprocessor technology, which soon became the high-profit path to the future.[134]

6.3.2.2. India

India's rapid economic development started in 1991, when it opened to the world economy. Since then, its growth has been phenomenal. India's "Grey Revolution" is now focusing on knowledge and human brains, lead by the rapid increase in software development. Starting from the level of 3.4 million university students in 1985, twenty years later, in 2005, about 10.3 million students were enrolled in universities. About 350,000 of these were in engineering. By the year 2015, India is expected to have 18.5 million students enrolled in universities, 1.4 million of which will be in engineering.[135] Today, about 600,000 people in India work in software production. The Indian Semiconductor Association (ISA) estimates that the value of embedded software development exports were USD 4.9 billion in 2007, and that the embedded software market currently employs 106,000 engineers.

Gartner now expects India's ICT market to grow at a five-year compound annual growth rate of 20.3 percent and to reach USD 24.3 billion by 2011.

India has rapidly grown to be a major hub of semiconductor design. According to a joint study by Indian Semiconductor Association and IDC, the total ICT design market in India was USD 6 billion in 2007, and it was expected to grow to 7.37 billion in 2008.[136] Embedded software was the largest segment, with 81 percent of revenues, followed by very-large-scale integration (VLSI) design, at 13 percent, and hardware/board design contributing 6 percent. The number of employees working in India's design industry is estimated to be 130,000.

The largest pure-play IP company is Ittiam Systems, which focuses on advanced media communication applications for which software solutions are either unavailable or too expensive. Another pure-play IP firm, Cosmic Circuits focuses on analog circuits. Cosmic Circuits claims that that it has developed over 75 IP cores for applications such as power management, video analog front-end, and WiMAX and WLAN front-ends, and that it is able to create cores from 350 nm to 65 nm processes. The leading global provider of WLAN and Bluetooth IP is Wipro-NewLogic, which was formed when the Indian design service giant Wipro acquired the Austrian New Logic for USD 56 million in 2005. Other design service firms, such as Mindtree and Sasken also now develop their own semiconductor IP.

In-Stat estimates that the Indian design services industry will grow from USD 1.4 billion in 2007 to 3.4 billion in 2012, at the compounded annual growth rate of 20.2 percent. The Indian Semiconductor Association (ISA), in turn, estimates that the revenues from VLSI design services in 2008 will be about USD 927 million, and expects the combined IC design and embedded software industry to grow to USD 43 billion in 2015. Today, design services are dominated by the captive design centres of multinational companies. In 2007, the contribution of the captive centres was 54.7

134 For a discussion and further references, see Langlois & Steinmueller (1999).
135 Mashelkar (2008).
136 ISA-IDC (2008).

percent of the total revenues. At present, most of the leading semiconductor firms have established design centres in India, including Texas Instruments, Intel, STMicroelectronics, Freescale, AMD, Infineon, NXP, Cypress Semiconductor, Nvidia, Xilinx, Virage Logic, Analog Devices, and ARM. Also major electronic equipment producers, such as Nokia, Samsung and Motorola have established design centres in India. Intel had about 2,900 R&D workers in India in 2006, Texas Instruments about 1,300, Motorola 1,500, Cisco 1,000, and one of the leading EDA firms, Cadence, about 500.[137]

The estimated number of IC design starts in India was 516 in 2007. In-Stat expects the number of design starts to grow to 1,305 in 2012. In 2007 about 40 percent of the design starts were for 90 nm process, and about 20 percent for 65 nm process. By 2010, the leading process node in India will be 65 nm, with about 30 percent of design starts, according to In-Stat. By 2012, about 32 percent of new designs are expected to be for 45 nm and below. ASICs constituted about half of the design starts in India in 2007, while about 22 percent were for Systems-on-Chip and about 17 percent for FPGAs.[138]

The geographical diffusion and concentration of IC production has been studied extensively during the last decades, also because policymakers have perceived the industry as a key to the future information society. The history of Silicon Valley has inspired many attempts to create high-tech clusters in other parts of the world. Many of these attempts have failed because the emergence of Silicon Valley has, indeed, been a historical process in a context that is impossible to recreate. This, of course, does not mean that it is impossible to learn from this history. Indeed, the recent ecosystem based approaches have been based on the idea that a complex system of complementary actors and their co-evolution are needed to create efficient locations for knowledge-intensive production. Today, however, it is not obvious that such ecosystems need to be based on physical proximity, and examples of Internet-supported ecosystems exist.

The rise of the Asian Tigers, in turn, highlight the fact that the semiconductor industry became a globally networked industry in the early 1990s, following an earlier phase of internationalization led by US firms. Silicon Valley, itself, could not exist today without its extensive links to Asia. Following the model provided by Japan, the Asian Tigers joined the global economy based on highly successful export oriented national policies, supported by competences developed mainly in the leading US universities and semiconductor firms. Gradually, the Asian Tigers climbed the value chain toward high-value adding activities, developing regional ecosystems that effectively support specific segments of IC production. Today, countries such as South Korea explicitly aim at moving beyond the state-of-the-art, to the next emerging levels of value production, focusing on, for example, broadband mobile and ubiquitous systems, and related systems-on-chip.

India is a latecomer in the industry, and it has very rapidly become a major focal point for software and design services. Yet, it still does not have chip fabrication facilities. This is often explained by the fact that the country still lacks reliable infrastructure. As one industry researcher puts it, there is too much dust in India. Although the country has many excellent universities, the differences in the quality of education vary greatly. The dream of many well-educated Indian ICT workers is to move abroad. This is in great contrast with China, where the Confucian educational principles aim at educating all citizens and where many professionals dream of a future where they can work for leading Chinese firms. Due to China's potential relevance for the future of European semiconductor IP industry, we discuss the Chinese IC design and IP activities in a separate chapter.

137 Mashelkar (2008, 154).
138 Lohyia (2008).

7. Makimoto Waves, Dominant Designs and User Innovation

For industry participants, the semiconductor industry has been a difficult industry because of its cyclical nature. New manufacturing capacity requires large investments, and competing firms tend to invest when business prospects look good. This has regularly led to overcapacity and periods of low profitability. Rapid technical advances in the industry also mean that opportunity windows are narrow and research and development costs are often recuperated and profits generated in the first months of product availability. Semiconductor manufacturing is further characterized by very steep learning curves that provide large competitive advantage for first entrants. This combination of large swings in business cycles and rapid obsolescence of old products and production technologies makes the semiconductor industry a rather exceptional industry.

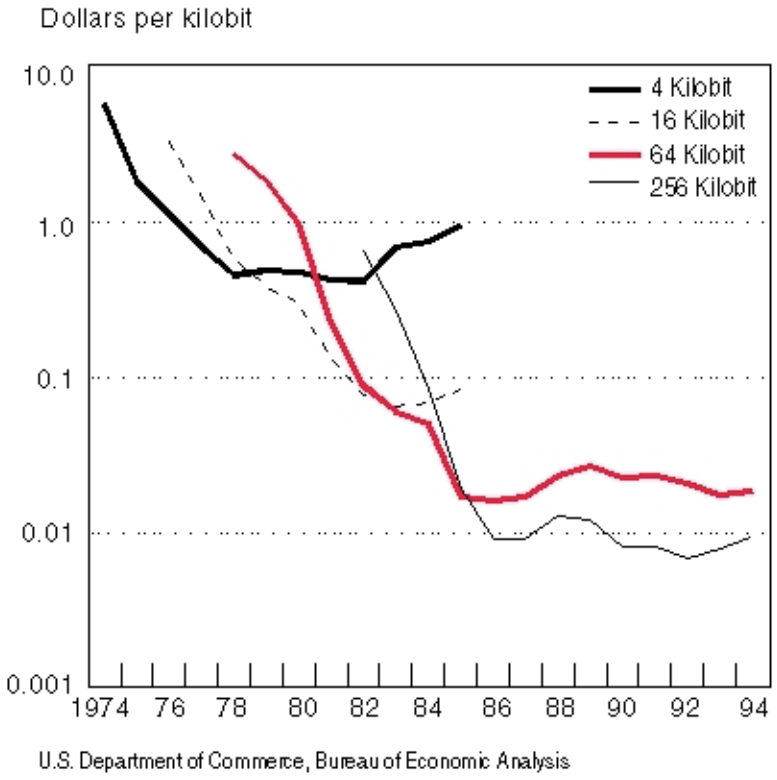
In this chapter, we first briefly describe the characteristics of learning curves that drive the development of high-volume products such as dynamic random access memories (DRAMs) and general purpose processors. The following section then discusses historical industry cycles between standardization and customization, known as Makimoto waves. We also extend the Makimoto model in an attempt to propose some potential future developments in the industry and in its product architectures, for example, by taking into account the end of scaling. The following section then puts the discussion in a broader context of technology maturation, arguing that processing architectures are entering a technology maturation phase where dominant and optimized designs are increasingly being replaced by user-centric product designs, and that configurability is becoming increasingly important for future integrated circuit designs. We present a simplified model of technology maturation and its innovation drivers to provide some starting points for further discussion. Although the model is only a first sketch of a complex reality, and should be refined and justified by empirical data, the key argument in the present context is that the emergence of new innovation and product development models will imprint their requirements also on integrated circuit architectures. In the future, learning is no more confined to the industry itself; instead, processing architectures are becoming innovation platforms for end-user industries and, eventually, for user communities. This will introduce first configurability and then reconfigurability as new key industry drivers, making the Makimoto dichotomy between standardization and customization increasingly obsolete.

7.1. Learning and Obsolescence in the IC Industry

Although leading-edge integrated circuit technology typically is more expensive at introduction than the previous generation technology, rapid improvements in high-volume leading-edge technologies usually make earlier technologies quickly obsolete. Historically, the semiconductor industry has been characterized by very steep learning curves that rapidly erode the competitiveness of old technology generations in application areas where technical performance is important. As technical performance was associated with scaling, which implied simultaneous improvements in product cost, performance and size, traditionally there has been little profitable space for manufacturers who have not upgraded to the leading-edge. More recently, the shrinking life-time of consumer products has intensified this time-focused mindset in the industry.

The typical price dynamics of semiconductor chips is shown in Figure 26, which depicts the

Figure 26: Price dynamics in different DRAM technology generations, 1974-1994



Source: Grimm (1998).

prices of storage bits in Dynamic Random Access Memory (DRAM) chips for several product generations.[139] As can be seen in the figure, the introduction price for new generation chips is higher than the current price of more mature chips, but the next-generation technology rapidly becomes cheaper. Towards the end of the product cycle, the price decline stops, as the product generation becomes a niche product.

In the last three decades, new DRAM product generations have entered the market in about every two years, on average. The profit windows are measured in months and the difference between profit and loss sometimes in weeks.

For example, between December 2006 and April 2007, the average selling prices for DRAM chips dropped about 33 percent, according to Semiconductor Industry Association (SIA) data. This means that the value of products in the manufacturer's or seller's inventory drops more than one percent each week. The industry, therefore, can be characterized as a "fish business," as the products on the shelf begin to stink if they are not moved to end-users fast enough.[140] Although new business models are emerging, this historical fact of extremely fast obsolescence underlies the industry's dominant logic.

The learning curves shown in Figure 26 represent the impact of several key factors.[141] Dedicated process development facilities, geographic proximity between development and manufacturing facilities, and the duplication of equipment between development and

139 Grimm (1998, 13).

140 The fish business analogue comes from the hard-drive industry (McKendrick, Doner, and Haggard 2000, 30).

141 Hatch and Mowery (1998).

manufacturing facilities have all been historically important factors in improving performance in introducing new technologies. All these have to do with knowledge transfer, and, in particular, transfer of tacit knowledge.[142] Semiconductor manufacturing processes are complex interdependent configurations of sub-processes and process steps, where relevant parameters are sometimes empirically found and optimized. Although it may be possible to specify how the different process steps have to be done in a given production context, it is very difficult or impossible to define optimal processes in generic terms. Successful ramp-up of production, therefore, depends on the effective transfer of unarticulated contextual knowledge from development facilities to production.

Historically, this has meant that research and development of new chip technology and its manufacturing have been co-located. Intel has extended this approach using its "Copy Exactly" methodology, where manufacturing facilities are built as detailed copies of development facilities. In this approach, the firm first creates and optimizes the production process in a development fab and then makes identical copies of the optimized process in other locations.[143] Contextual knowledge is transferred, for example, by copying the plant layout, lengths of water pipes, instrument settings and configurations, as well as other process parameters.

7.2. Cycles of Standardization and Customization

Technical advances and steep learning curves have enabled new functionality to be implemented at constantly declining costs in the integrated circuit industry. This has constantly pushed the technology frontier towards new product generations. At the same time, the point of gravity in the industry has moved between standardized and customized products. One expression of this idea is the so-called Makimoto Wave. Originally devised by Tsugio Makimoto from Sony in 1991, the wave is a model of ten-year cycles in the semiconductor industry between standardization to customizability.[144]

According to Makimoto, the semiconductor industry swings like a pendulum between customization and standardization. When many new devices, architectures and software innovations appear, the semiconductor industry as a whole moves towards standardization. As standardization becomes an increasingly dominant trend, need for product differentiation and added value start to act to the opposing direction of customizability. Amplifying this counteraction is an imbalance between supply and demand, as overcapacity develops for dominant standard products.

When new developments in design and manufacturing technologies catch up with the possibilities of the underlying semiconductor technologies and enable increasingly complex designs, product customization becomes an increasingly dominant trend. As customization starts to dominate, this trend, in turn, is slowed down by the need to lower product cost and to improve operational efficiencies is manufacturing. Further, as products are customized and require more design effort, time-to-market becomes an increasingly important source of competitiveness. This "Makimoto pendulum" is depicted in Figure 27.[145]

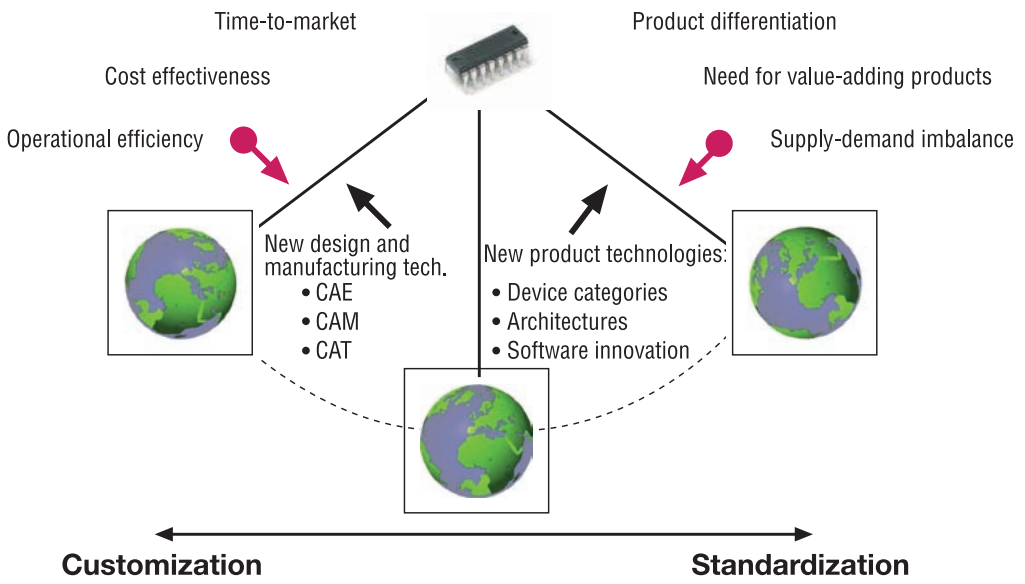
142 Tacit knowledge includes contextual and non-articulated knowledge. The concept originates in Michael Polanyi's works, e.g. (Polanyi 1967), and was popularized by Nonaka through his knowledge creation model (Nonaka 1994).

143 Cf. Chesbrough (2003, 113-33).

144 Makimoto (2003).

145 The picture is based on presentation by Makimoto at the IEEE Field Programmable Technologies Conference held in December 2002 in Hong Kong. We have rewritten Makimoto's explanation and some of the terminology.

Figure 27: The Makimoto pendulum



Source: Meaning Processing.

The swings of the Makimoto pendulum creates cycles as shown in Figure 28, where we have added two cycles to Makimoto's original model.[146] In the mid-1990s, for example, the number of new application specific integrated circuit (ASIC) designs totalled probably more than 10,000 each year. Each top-tier ASIC provider could count almost two new designs for every working day.[147] Since then, the focus has shifted from customization to standardization, first to application specific standard products (ASSPs), and, more recently, to customer configurable hardware, especially to field programmable gate arrays (FPGAs). According to a recent estimate, there has been a 40 percent decline in new ASSP/ASIC design starts during the last four years.[148]

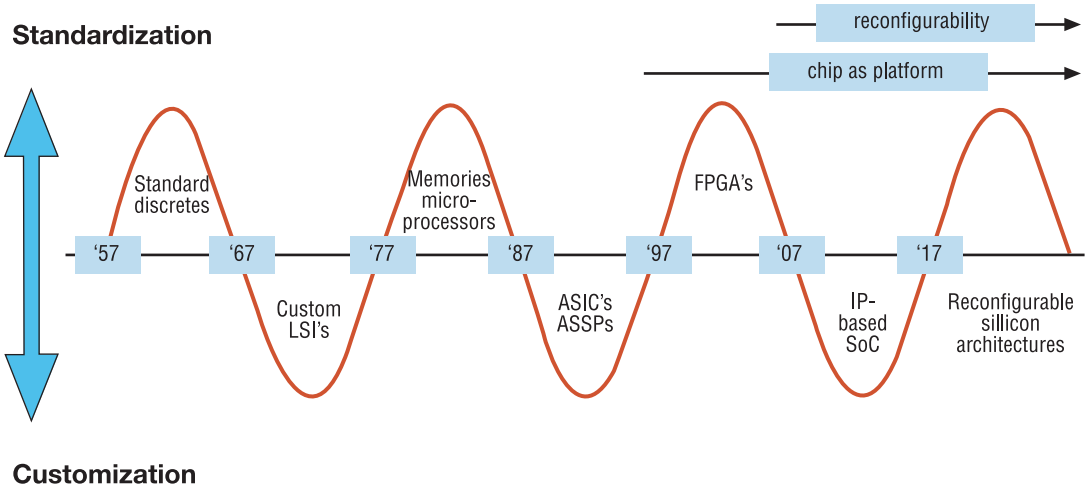
In year 2008, Gartner Dataquest expected ASIC and ASSP design starts to continue to fall to reach 7,500. In contrast, the design starts for FPGA was expected to reach about 90,000.[149]

In the Makimoto model, the cycles of customization and standardization are defined from the point of view of the semiconductor device industry. For the early history of the industry, this point of view is quite unproblematic. One should note, however, that as devices become increasingly complex, also standardized products can be highly customizable from the end user point of view. In Figure 28 we have followed Makimoto's original logic and located ASSPs on the customization wave and FPGAs in the standardization wave.

ASSPs are, in fact, technically ASICs. The difference between ASICs and ASSPs is not

146 The model is obviously a heuristic model, and it is not obvious how it could be empirically verified. For example, the y-axis dimension is undefined in the model. In the first approximation, one could try and interpret it as the production volume of the dominant product category in a given period.
147 Selburn (2004).
148 Manners (2008).
149 Data from a presentation by Jim Tully at Design & Reuse IP08 Conference, December 2008, as quoted in Pele (2008b)

Figure 28: Extrapolated Makimoto waves, 1957-2020



Source: Meaning Processing.

technical; instead, it is in the business model. ASSPs are sold in large volumes for many similar customers who do not try to differentiate their end products based on a proprietary chip design. For example, many mobile phone manufacturers and set-top box makers now use standard chip platforms that are built on ASSPs. ASSPs may, therefore, be understood as a product category that extends the swing of the Makimoto pendulum beyond the limits of ASICs, when cost, time to market, and operational efficiency start to make customer-specific ASICs uncompetitive. In a somewhat similar way, chip architectures where only some upper layers of the chip are left for customer configuration and most layers are mass-produced, known as "structured silicon," try to push beyond the cost, time to market, and operation efficiency boundaries.

FPGAs, in turn, are standard products from the manufacturing point of view. From the end user point of view, they, however, are customizable, and can be loaded with basically any digital functionality that the user wants. Modern FPGAs are also reconfigurable, and their logic circuitry can be reprogrammed, for example, over the Internet.

Whereas the original Makimoto pendulum was driven by the underlying continuous improvements in technology and by normal competitive forces, including time-to-market, cost effectiveness, operational efficiency, product differentiation, need for value creation, as well as industry-level cycles of overcapacity, the future developments in the industry will also depend on emerging new dynamics of innovation. For end-user industries, integrated circuits are increasingly used as innovation platforms. Chips that have processing capabilities do not necessarily completely define product functionality, which becomes gradually defined during the life-time of the product. In Figure 28 we note this development towards looser coupling between the chip design and product design by adding two new trends –"chip as platform" and "reconfigurability"– to the picture.

The first of these refers to the case where the chip architecture provides capabilities and options for product evolution. A relatively straightforward approach is to create full programmable systems-on-chip, where application-level software can be used to change chip functionality. This is basically the current IP-based approach, where pre-designed IP blocks are configured into a

full programmable system on a chip. The main attraction of this approach is that if processing can be done using general purpose processors, the system can be programmed using standard software programming languages and tools. The swing from FPGA's to IP-based SoCs is enabled by customizing pre-designed and standardized design blocks. It thus requires the existence of a robust IP vendor population, system-level design tools and a new level of design abstraction.

An extension to this IP-based SoC wave is to create reconfigurable hardware, for example, by including FPGA blocks on the chip. When FPGA-based configurability is combined with specialized IP-blocks that, for example, process multimedia data streams, efficient and high-performance systems can be built using a single chip. In this approach, customization is based on combining function-specific processing blocks and modifiable components, which can be manufactured in standardized processes.

Beyond the IP-based SoC wave, the swings of the Makimoto pendulum may become somewhat chaotic, as new forces come into play. As the marginal cost of increasing the number of transistors grows, it becomes increasingly expensive to waste transistors on a chip. This means that designs have to be increasingly hardware-aware, and generic software-based solutions become inadequate.

In particular, the end of scaling implies that there is only limited space for future improvements in conventional FPGA technologies, as improvements require increases in the number of transistors on a chip. FPGAs have benefited greatly from the declining costs of components on a chip and the fact that during the last decade the absolute number of these components became so high that very complex functionality can now be configured on a single chip. The basic challenge, however, is that the fine-grain granularity that makes the implementation of any logic circuitry possible on a FPGA makes them sub-optimal for almost all applications. The flexibility of FPGAs also means that their power consumption is usually very high compared to more optimal processing architectures. As more and more digital devices are used, both the overall energy consumption in the society and the battery life-time of mobile devices become increasingly important considerations, thus reducing the attractiveness of FPGA architectures.[150]

As new open and continuous innovation models penetrate IC user industries, products are increasingly designed as flexible platforms for continuous evolution and improvement. Product reconfigurability thus becomes increasingly important. Standardization, in turn, is –in addition to manufacturing cost– pushed by the fact that many future products will include embedded processing and communications capability and products will be interconnected. A relatively straightforward extension of the Makimoto trajectory would, then, lead to heterogeneous IC architectures that have flexible reconfigurable processing cores and interface components that can be configured for standardized communications and interaction protocols. A basic challenge is to create low-cost products that can be both customized and dynamically reconfigured using high-level functional descriptions and tools.

One early example of a product that moves toward this direction is the "software defined silicon" chip introduced by XMOS in 2008. The XMOS architecture –which is inspired by the earlier Transputer architecture developed by Inmos in the UK in the 1980s– essentially provides a set of parallel processing units that can be programmed and configured to a specific architecture using a software program. A more application specific example is the Montium reconfigurable digital

150 Although it is possible that radical new approaches, such as FPGAs based on spintronics, could make FPGA architectures viable also in the future, at present it is not known what these radical approaches would be or how they could be implemented.

signal Tile Processor, developed by Recore Systems, based in the Netherlands. The Montium processor is configured by loading an application-specific set of instructions to its processors and by configuring the data paths according the needs of the task at hand. Whereas the XMOS architecture is based on programming a set of processors and combining them in a way that solves the computational problem at hand, the Recore architecture is based on modifying the actual set of instructions that the underlying parallel processors handle. The Recore architecture also assumes that the data can be processed in parallel without referencing data that is "distant" in time or space from the currently processed data. This makes the Recore architecture suitable for typical multimedia streams, including video processing. Both architectures can be manufactured as large-volume chips, yet they allow customization and reconfiguration by the users.

Whereas the underlying dynamics and predictive value of Makimoto's Wave model can be debated, it highlights the point that the sources of profitability change as technology advances. As Makimoto focused on the dynamics of semiconductor manufacturing, the key drivers in his model only implicitly take into account the demand structure and end-user requirements. The model also does not explicitly describe the trends of the drivers themselves. For example, an important factor in the recent decline in ASIC design starts has been the increasing fixed cost of new designs, combined with the technical and business risks associated with complex designs in leading-edge technologies and shrinking end-product lifetimes. Whereas time-to-market and cost efficiency remain key drivers in the industry, the escalating costs and tighter opportunity windows slow down the swing of the Makimoto pendulum, almost as if the gravitational constant would be increased over time.

An important factor in the upswing of the pendulum in the standardization cycle is that new innovations in fundamental technologies tend to generate many attempts to benefit from the emerging possibilities. This point is supported by empirical studies on technology innovations. A broader view on the dynamics of semiconductor industry can therefore be gained by looking at the typical patterns in the development of technical products.

7.3. Configurability and Recombination

When a new promising technological opportunity emerges, it creates a large number of product ideas and a large variety of products.[151] Abernathy and Utterback called this stage the "fluid phase" of innovation.[152] This phase typically leads to a "transitional phase" in which the rate of major product innovation slows down and the rate of major process innovations speeds up. At this point, product variety begins to give way to standard designs. As the form of the product becomes settled and a dominant design emerges, the pace of product innovation slows down and the intensity of process innovation increases, leading to declining costs and optimized performance. Some industries enter, according to Abernathy and Utterback, a "specific phase," in which the rate of major innovation dwindles for both product and process. These industries become extremely focused on cost, volume, and capacity, and innovation occurs in small incremental steps.

Why such a developmental path emerges? In current terminology, one explanation is that an ecosystem forms around the most attractive product feature configurations, leading to the emergence of a dominant design. In this phase of technology maturation cycle, the dominant design provides a definition of what the product is and where it belongs in the

151 Schumpeter (1975) described this as the "swarming" of entrepreneurs. The impact of this process on the rate of innovation and firm entry and exit was first explored by Mueller and Tilton (1969).

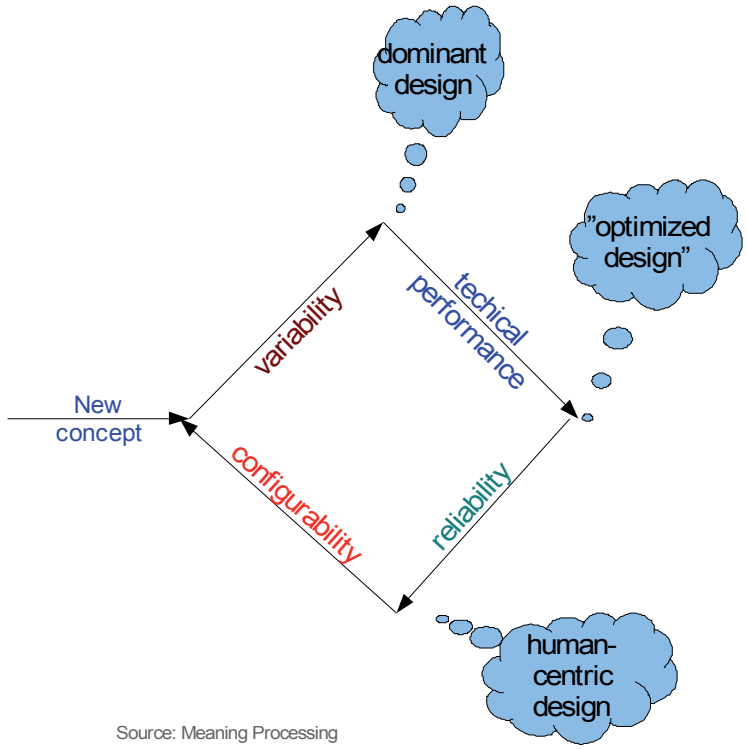
152 Utterback and Abernathy (1976), and Utterback (1994).

ontology of ecosystem actors. The dominant design therefore allows multiple actors to link and stabilize their interactions with each other and the focal product. The ecosystem actors also span an interlinked net, increasing the difficulty of changing the dominant design, except through gradual evolution. To give an example, the historical emergence of the QWERTY typewriter keyboard as a dominant design required the establishment of training providers that had courses standardized on using the QWERTY keyboard.[153] In addition, it also required competent writers who had invested their time and effort in learning to use the keyboard. As the actor linkages stabilize, technical improvements, on the other hand, can be evaluated in this context and dominant lines of improvement emerge. Technical improvements then further lead to a current "technically optimized" design, which effectively and efficiently implements the main characteristics of the dominant design.

Technical optimization results in high-performance products that are best adapted to those users that prioritize technical performance at any feasible cost. In the early history of integrated circuits, the US military was such a user. Technical optimization, however, leads also to product variants that optimize technical performance in relation to product cost. In this model, advancing technology makes the purely performance-oriented user segment eventually a minority. As the performance-price relation is good enough, the majority of users start to focus

153 QWERTY typewriters are commonly used as examples of dominant designs. This example, of course, is somewhat culturally biased as, for example, French speaking countries do not use QWERTY keyboards.

Figure 29: Innovation drivers in new product categories



Source: Meaning Processing.

on other criteria, including product reliability and ease of use. This leads to an increasingly "user-centric" and human-centric emphasis on product improvements. At that point, engineering knowledge is increasingly complemented by cultural and social knowledge when products are designed.

Figure 29 shows such a generic model of technology maturation.[154]

The concepts of "ease of use" and "user-centric" require, however, some further consideration. The common idea that product characteristics can define products that are "easy to use" implies that product uses are predetermined and stable.[155] The "users," in this conceptualization, represent a dominant segment of users. In practice, this model works best when production is organized as mass-production, as it often was in the 19th century. In reality, however, there are usually many different communities of users. The "same" product is used in many social practices, and each community of practice constructs the meaning of the product from its own point of view. When the product becomes sufficiently reliable and usable, these different user communities start to reinterpret the possibilities of the product functionality and technology, in effect reinventing the product characteristics using the current functionality as a starting point. At that point the product becomes a platform for user-centric innovation. The configurability, flexibility and modifiability of the underlying product, then, become increasingly important. This dynamic is visible, for example, in the mobile communications industry and in the evolution of the World-Wide Web.[156]

In the above model, the different phases of product maturation and renewal are driven by different value propositions, and the locus of innovation also shifts between the phases. Different types of knowledge are needed and different sources of knowledge and innovation become focal in the different phases. In particular, when a dominant design is optimized, progress is typically measured using engineering criteria established by the industry that produces the product.[157] When product configuration becomes the dominant driver, the criteria established by innovative users become more central.

The importance of configurability as an enabler of end-user innovation has been widely recognized in recent years. The role of configuration and recombination is highly visible in the software domain, where the growth of the Internet is to a large extent related to the combinatorial mode of innovation, where existing technologies are reconfigured and adapted to new innovative uses.[158] In this regard, hardware innovations such as IC designs are not different from software. The relative invisibility of the combinatorial growth mode in semiconductor hardware has to a large extent been related to the fact that semiconductor design has required specialized knowledge and access to expensive tools and implementation

154 The model extends earlier research on technology evolution by Christensen *et al.* (Christensen 1997; Bass and Christensen 2002; Rosenbloom and Christensen 1994; Bower and Christensen 1995) and Utterback (Utterback and Abernathy 1976; Utterback 1994), along the lines of the downstream distributed innovation process model by Tuomi (2002a). Dominant designs emerge here when many stakeholders form a network of interests that slow down developments in the focal product. This variation of the dominant design concept is particularly suitable for system innovations, where the focal product forms a key subcomponent. Programmable integrated circuits are examples of such subcomponents.

155 The concept also works best when only entry-level users, i.e. new product buyers, are considered. Ease of use means very different things, for example, for a novice musician and a professional violin player but we rarely think that violins are badly designed because everyone can not play them well.

156 Tuomi (2002a; 2005).

157 This is particularly the case when the innovation ecosystem is dominated by the focal developer community, which establishes its evaluative criteria as the measure for improvement. See Constant (1987).

158 The combinatorial mode of innovation and its role in the development of Internet technologies is elaborated in Tuomi (2002a, chap. 7).

systems. As the technical performance of information processing technologies becomes sufficient for the majority of potential users, in the model presented above the main bottleneck for innovation shifts to social and economic entry barriers that potential innovators face. Lowering these entry barriers, therefore, could lead to a very rapid expansion of innovative activity in semiconductor hardware and close-to-hardware software.

A more fundamental challenge and opportunity is related to the entry point in Figure 29. If the integrated circuit technology has evolved according to the phases described above, could a new cycle be created using fundamentally new concepts of computing?

Although computers are used in all areas of life today, current computing models work optimally in only few special cases. These special cases are extremely important in practice, which is one of the reasons why the present-day computing models have successful been used since the 1940s. The stored-program algorithmic computing models, used in almost all microprocessor-based computers and programmable devices, however, were originally intended to solve two basic kinds of computational problems: iterative solution of differential equations, and syntactic manipulation of character strings.

The first application area was related to physical computations, including artillery trajectories. The second application area was originally related to decryption of encrypted messages, and later, to storing character strings for census data, payrolls, and other similar database applications that underlie the social organization of the Information Society. Although computers have been used for many applications beyond these prototypical cases, many of these are inherently incompatible with traditional computational models and require brute-force approaches that lead to escalating computational requirements.[159] The common belief, according to which we today have sophisticated computational architectures, therefore, is to a large extent based on an illusion that has survived because the rapid scaling of integrated circuits have brought with it rapidly increasing computational performance. In practice, however, much of the sophistication in the underlying processing and chip architectures is aimed at overcoming and mitigating technical challenges created by the limitations of the underlying models of computation.[160]

One interesting possibility for future IP processing architectures, therefore, could be that new ecosystems form around new paradigms of computing. For example, real-time embedded systems require new computational models and programming approaches that may considerably differ from the conventional approaches.[161]

159 Today, algorithmic computation is successfully used, for example, to model wind-tunnels. The trade-offs between analog computing using wind-tunnels and digital computing were not obvious in the early history of computing, and the were analyzed insightfully by Wiener (1975). In general, the algorithmic approach becomes increasingly tedious when computational problems cannot be reduced to context-independent calculations. Differential equations and syntactic manipulation of character strings belong to a special class of problems where context does not matter. Algorithmic computations work particularly well for solving problems in Newtonian mechanics, as context-independence is a basic feature of the Newtonian physics, which is also reflected in the fact that Newton's equations can be represented as simple differential equations. In most real-world problems, such as weather prediction, natural language processing, artificial vision, and real-time embedded systems, the standard computational model leads to fundamental challenges. These challenges present themselves, for example, by the fact that almost all computational problems lead to exponential growth of computational complexity.

160 For computing professionals, the fundamental theoretical limitations of common computational models are also sometimes obscured by the fact that stored program algorithmic machines are known to be related to universal Turing machines. The nature of universality is often misunderstood, however, as Turing machines are formal mechanistic procedures that exist in a world that does not have external interactions, time, or space. Universal Turing machines are universal because they end their computations for all algorithmically computable tasks after a non-infinite sequence of steps. In the real world, many problems require infinite time to define with sufficient accuracy the computational problem in a form that the universal Turing machine could then compute. This was called "the starting problem of Turing machines" in Tuomi (1988).

161 See, for example Lee (2008).

Locations that have relatively low cognitive, educational and economic investment in the prevailing paradigm could well be able to leapfrog relatively easily to the next generation information and meaning processing models, as the end of scaling makes progress in the old paradigm increasingly difficult. An interesting possibility, for example, is that China could enter the IP arena in this fashion.

8. China as a Creator of Future Intellectual Property Architectural Blocks

In this section, we provide an overall view of the recent developments in the semiconductor sector in China, and discuss in more detail IC design activities and semiconductor IP in China.

8.1. The State of the IC Market

China has rapidly emerged as a global leader in the electronics and semiconductor industry. In year 2006, it produced 480 million mobile phones, 93 million microcomputers, and 33.6 billion integrated circuits. In year 2007, it produced 517 million mobile phones, 120 million microcomputers and 41.2 billion integrated circuits.[162] In 2007, China's semiconductor market became a 88.1 billion USD market and it now accounts for over one-third of the world's total. As a consumer of semiconductors, China is over two times bigger than Europe or North America. Although in 2007 almost 6 percent of the growth resulted from currency exchange rate changes, the Chinese semiconductor market has been growing much faster than in the rest of the world. Since 2001, China's semiconductor market has grown at a 31.5 percent compounded annual growth rate, while the worldwide market has grown at a 10.6 percent rate. In 2007, the Chinese consumption for optoelectronics, sensors, and discrete semiconductors was USD 14.2 billion, and the integrated circuit consumption was 562,373 million Yuan, or about USD 73.9 billion, growing 24 percent from 2006.[163] During 2007, the Chinese IC consumption increased by USD 14.4 billion while the worldwide IC grew by USD 9 billion. According to PricewaterhouseCoopers 2008 update on China's impact on the semiconductor industry,[164] this indicates that the Chinese market grew by displacing consumption in other regions. According to data from China Centre for Information Industry Development (CCID) Consulting, the expansion is Chinese IC market is, however, slowing down. Since 2003, the annual growth rate has slowed down from 41 percent to 18.6 percent in 2007. In the first half of 2008, the sales revenue growth declined to 11.8 percent from the first half of 2007.

The rapid growth of the Chinese semiconductor market has been driven by the global transfer of electronic equipment production to China. Whereas China produced about 9 percent of electronic equipment in year 2000, in 2007 it produced already 27 percent.[165] The semiconductor content was also higher in electronic equipment produced in China than in the rest of the world. The largest suppliers to the Chinese market are the leading international semiconductor firms. In 2007, Intel had a market share of about 14 percent, followed by Samsung (5.4%), Hynix (3.9%), Texas Instruments (3.4%), Toshiba (3.3%), AMD (3.1%), NXP (2.8%), and STMicroelectronics (2.7%).

To a large extent, the consumption of chips in China is based on exports of electronic products. The rapid growth of manufacturing finished electronics products was the main source of the rapid growth of semiconductor consumption in the first half of the decade. This expansion started to slow down in 2005, leading to slower growth rates of Chinese IC markets. According

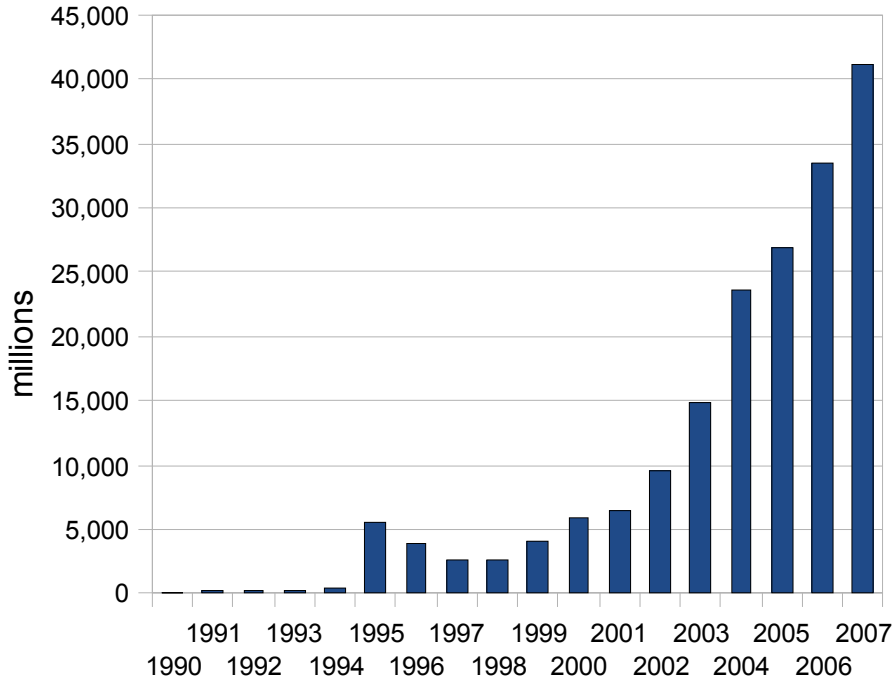
162 Data from China National Bureau of Statistics and China Center for Information Industry Development (CCID) Consulting. NBS integrated circuit statistics report "pieces" produced, and the actual definition depends on the type of producer. The numbers, therefore, cannot be directly interpreted as the number of final IC products. For a discussion, see Pausa et al (2008), Appendix 1.

163 CCID and Pausa *et al.* (2008).

164 Pausa *et al.* (2008).

165 Pausa *et al.* (2008).

Figure 30: Production of integrated circuits in China, 1990-2007



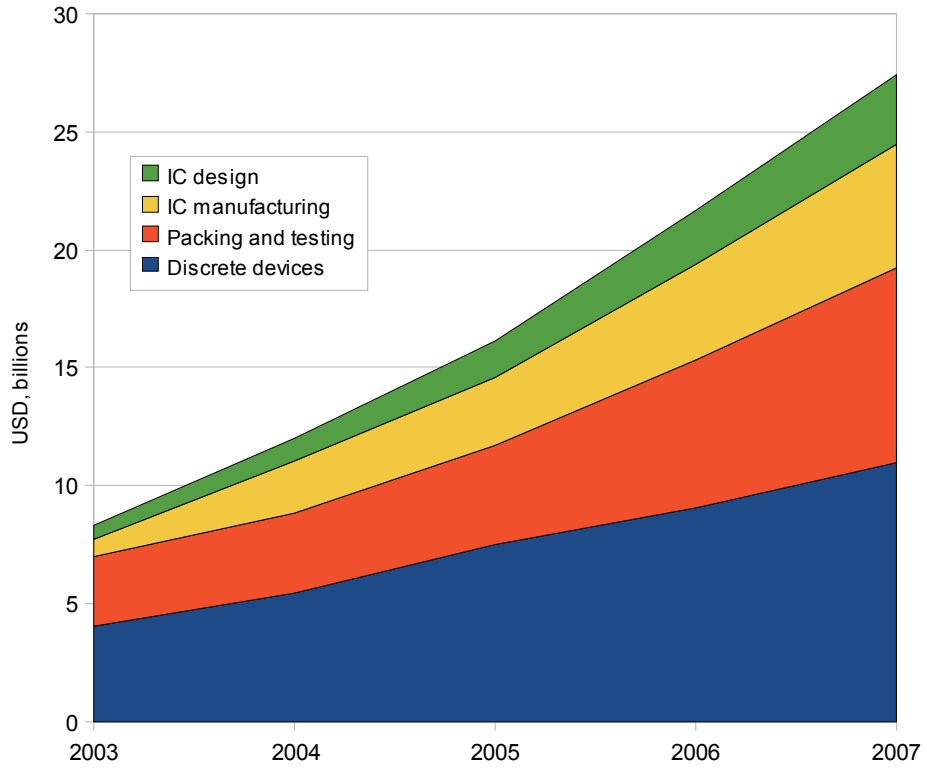
Source: National Bureau of Statistics of China, various years.

to the PricewaterhouseCoopers (PwC), about 69 percent of total consumption was for products that were assembled in China and exported for sale in other countries in 2007.[166] This number, however, includes also semiconductor products that are actually bought outside China but transhipped to China. As PwC points out, some customers purchase semiconductors outside China for reasons such as supply chain management, intellectual property protection and toll processing business models. According to PwC, up to 48 percent of Chinese consumption was bought outside China. For example, many Taiwanese, Japanese, Singaporean and European electronics equipment manufacturers tranship components to China, where they are assembled into finished products. About two thirds of these products are then exported out from China. The total consumption of semiconductors in China, therefore, is both considerably larger than the consumption for local markets and also considerably larger than revenues generated by semiconductor producers in China.

Chinese semiconductor statistics, however, are not always easy to interpret. Foreign-owned and indigenous production are sometimes treated differently, and intermediate production is sometimes aggregated with final production, thus double counting essentially the same products. For example, PwC estimates that for many foreign-owned semiconductor packaging, assembly and testing (SPA&T) plants, the reported revenues may be about four times larger than they would be if reported using conventional reporting practices. This is because many foreign-owned firms sell the fabricated wafers to their Chinese SPA&T firms, and then buy back the assembled and tested chips. As a result, the Chinese statistics record the value of the final product also when only a fraction of the product value is added in China. Similarly, when different production steps are done by different companies, the Chinese statistics usually add the revenues of these companies to get the total industry revenue. The

166 Ibid, p.13.

Figure 31: China semiconductor revenues by industry sector, 2003-2007



Source: data from Pausa et al (2008), p. 21.

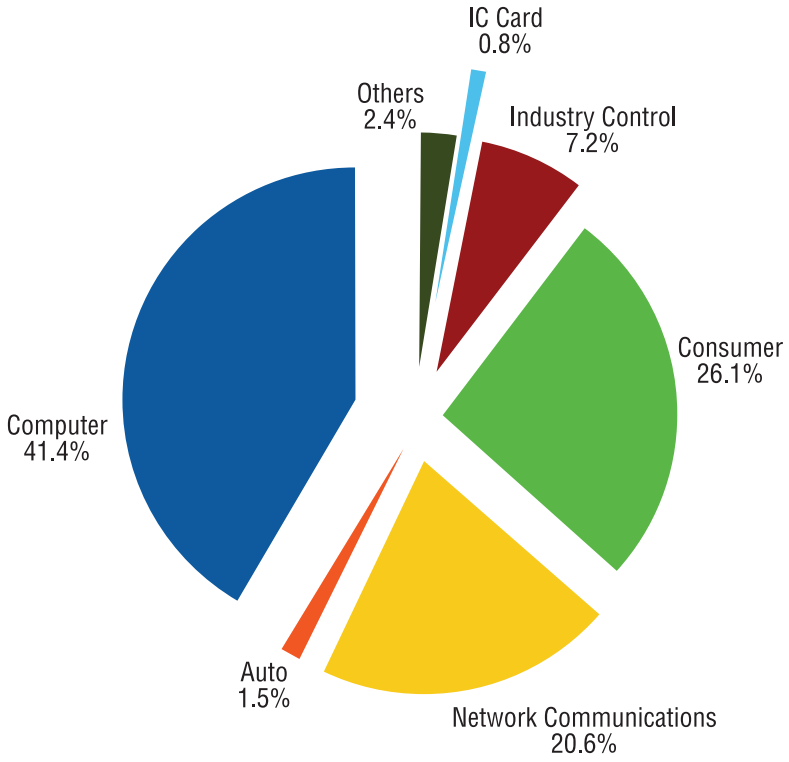
cost of wafers and their further processing steps, i.e., the revenues of intermediate producers, become added with the revenues of the finished product. It is therefore important to recognize that even the best available data on Chinese semiconductor industry is only indicative, and cannot always be directly compared with data on other countries.[167]

A key characteristic of the Chinese market is that, despite the rapid growth of production, China is still consuming considerably more semiconductors than it is producing. In 2007, the gap reached a record of USD 54.9 billion. This is one important reason for the Chinese policy makers to promote local production. The number of integrated circuits produced in China is shown in Figure 30, as reported by the National Bureau of Statistics of China.

Measured in US dollars, the reported revenues of Chinese semiconductor firms grew by 27 percent in 2007, reaching USD 27.4 billion. This includes the production of discrete semiconductor devices such as LEDs and transistors, packaging and testing, integrated circuit manufacture, and integrated circuit design. In China, the IC manufacturing sector includes wafer foundries, wafer fabrication plants of foreign-owned firms, and Chinese IDMs. The IC design sector, in turn, consists of IC design companies, institutes and laboratories, as well as all fabless firms. In year 2007, discrete devices were the largest segment, with 40 percent of the total, followed by IC packaging and testing (30.1%), IC manufacturing (19.1%), and IC design (10.8%). The growth of

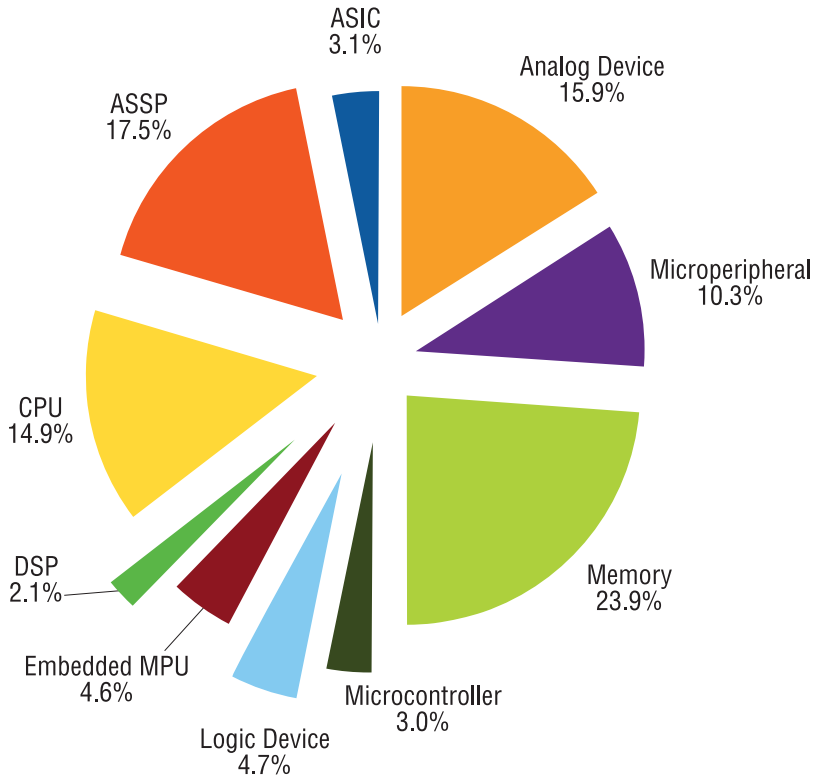
167 For a detailed discussion, see Appendix 1 in the PricewaterhouseCoopers' 2008 update on China's Impact on the Semiconductor Industry (Pausa, Gilhawley, and Wang 2008).

Figure 32: IC consumption by user segment in China, 2007



Source: CCID, 2008.

Figure 33: IC consumption by product category in China, 2007



Source: CCID, 2008.

revenues by industry sector in the 2003 to 2007 period are shown in Figure 31.[168]

The use of produced and imported ICs was dominated by computers, followed by consumer electronics and network communications. The customer structure of the Chinese IC market in 2007 is shown in Figure 32, based on data from CCID.

Consumption by product categories is shown in Figure 33.

Indigenous production still represents a relatively small fraction of the total semiconductor consumption in China. In 2007, the difference between Chinese IC consumption and production increased to USD 54.9 billion. Semiconductor consumption is also expected to grow faster than production in the next years. CSIA expects the China's IC market to reach USD 110 billion by 2010, when IC industry revenues are expected to be USD 33 billion. In local currency terms, CCID expects the IC market to grow to 1,238,400 million Yuan and production to 357,660 million Yuan by 2012. Using present currency exchange rates, this would imply a difference of about USD 128 billion, or almost half of the present semiconductor device market.[169] This growing production gap has prompted the Chinese policy makers to support initiatives and policies that aim at increasing indigenous production in the sector.

In fact, also much of the growth in the Chinese semiconductor production has been driven by multinational firms. From 2005 to 2007, China's reported semiconductor industry revenues increased from USD 16.1 billion to 27.4 billion, or about 70 percent, according to PwC.[170] The memory maker Hynix-Numonyx, originally a joint effort by Hynix and STMicroelectronics, contributed about 12 percent to the growth with the launch of its new fab in Wuxi. Qimonda followed with a contribution of about 11 percent, Freescale 9 percent, RF Micro Devices 3 percent, and Infineon with about 2 percent. The largest indigenous companies contributing to the growth during the two-year period were SMIC (2.1%) and Xinchao Group (1.7%), the former being now globally the fourth largest foundry with 2007 revenues of about USD 1.5 billion, and the latter being one of the leading packaging and testing vendors in China, with 2007 revenues of about USD 0.5 billion.

In general, multinational semiconductor firms have followed the historical pattern of first moving their most labour intensive activities to China. Among the top 20 semiconductor manufacturers in China, as listed by PwC,[171] Freescale, Qimonda, RFDM, Renesas, Panasonic, ST Microelectronics, Fujitsu, STATS ChipPAC, Infineon, Intel, and Samsung all have their main focus on packaging and testing. The main exception is the DRAM memory device maker Hynix-Numonyx, a wafer fab joint venture between Hynix and the STMicroelectronics and Intel memory spin-off Numonyx. Of the 50 largest semiconductor manufacturers in China, 24 focus on packaging and testing.

168 Data from CCID, CSA and PwC, as reported in Pausa *et al.* (2008, 21).

169 The Chinese IC market includes wafer fabrication, IC design, and semiconductor packaging, assembly and testing (SPA&T). It therefore consists of both sales of final products (the packaged chips) and intermediate production, such as wafer fabrication. The worldwide semiconductor market, measured as sales of final products, will be about USD 279 billion in 2008 according to Gartner November 2008 estimate.

170 On a local currency basis, this was 59 percent. Renminbi appreciated very fast in 2007 in US dollar terms, making USD conversions highly dependent on the actual exchange rate used. PwC uses the average annual exchange rate.

171 Pausa *et al.* (2008).

8.2. IC Design in China

In 2000, the State Council adopted the Policy for Encouraging the Development of the Software Industry and the IC Industry. Subsequently, the Ministry of Science and Technology approved seven national IC design bases in Shanghai, Xi'an, Wuxi, Beijing, Chengdu, Hangzhou and Shenzhen. At present, there are about 500 IC design enterprises across China.[172] The IC design industry generated revenues of about RMB 26.7 billion Yuan, according to CCID statistics, or about USD 3.5 billion.[173] Of the 491 design enterprises identified by CCID, about 390 are indigenous Chinese companies. According to PwC, the rest includes Chinese design activities of 18 of the top 25 multinational semiconductor companies and 24 of the top 100 semiconductor-consuming OEMs. The IC design segment represented 10.8 percent of the overall semiconductor sector in 2007. According to PwC, growth in this segment can almost solely be attributed to China's fabless companies, which in 2007 constituted about 6 percent of the worldwide fabless market.

IC design revenues have grown from USD 178 million in 2001 to over USD 3 billion in 2007, with a compounded annual growth rate of 60 percent. Measure in local currency, the year-on-year growth rate has declined from its 2003 peak of 108 percent to 21 percent in 2007.

According to data from Chinese Semiconductor Industry Association (CSIA), the top ten indigenous IC design focused semiconductor enterprises generated revenues of about USD 1.3 billion in 2007, as shown in Table 10. The leading firm, China Huada Integrated Circuit Design (Group) Co., Ltd. is a state-owned corporation specialized in IC design. It has about 600 staff with IC technology and management expertise. CIDC Group was formed in 2003 with partial funding from China Electronics Corporation (CEC) from the first Chinese IC design house, China Huada Integrated Circuit Design Centre, which was originally founded in 1986.

The second firm, HiSilicon, was established in October 2004, as a spin-off from ASIC Design

172 In its annual report on Chinese IC design market, CCID states that there are nearly 500 IC design enterprises across China. The China Semiconductor Industry Association IC Design Branch (CSIA-ICCAD) states that there were over 500 IC design houses at the end of 2007.

173 Using the year-and rate of 7.3 Yuan per US dollar, the revenues would have been USD 3.7 billion. The Yuan appreciated rapidly during 2007, and we get 3.5 billion using the exchange rate 7.6 Yuan per US dollar. PwC gives a lower estimate of USD 3.0 billion.

Table 10: Top 10 design houses in China based on revenues in 2007

Rank	Company	Revenue USD millions
1	China Huada Integrated Circuit Design Co. Ltd	240
2	Shengzen Hilisilicon Semiconductor Co. Ltd	186
3	Spreadtrum Co. Ltd	160
4	Datang Microelectronics Technology Co. Ltd	156
5	Actions Semiconductor Co. Ltd	127
6	Wuxi Huanrun Semico Microelectronics Co. Ltd	122
7	Hangzhou Shilan Microelectronics Joint-stock Co. Ltd	118
8	Vimicro Corp.	102
9	Shanghai Huahong IC Design Co. Ltd	98
10	Beijing Tshinghua Tongfang Microelectronics Co.	68

Chinese Semiconductor Industry Association (CSIA).

Centre of Huawei Technologies. HiSilicon claims to have IPRs of more than 100 types of self-developed chips and over 500 patents. At the end of 2007, it had over 1600 employees, two-thirds of them having a doctor or masters degree.

Spreadtrum, in turn, was incorporated in Cayman Islands in April 2001, and it established its wholly-owned subsidiary in Shanghai two months later. It is a fabless operation that focuses on wireless market. According to PwC, it had 576 employees at the end of 2007.

Datang Microelectronics Technology (DMT) is the former IC centre of China Academy of Telecommunications Technology. It specializes in smart card design, and has over 800 employees. Actions Semiconductor, in turn, focuses on SoC development for MP3 players and personal multimedia. It had 523 employees at the end of 2007.[174]

8.2.1. Design Capabilities

The growth of the number of IC design enterprises is shown in Figure 34, based on data from CCID. According to PwC, the number of employees has increased at least 10 percent between 2005 and 2007, and the number of enterprises with more than 100 employees was 21 in 2007. According to CCID, more than a third of IC design enterprises had less than 50 employees, and almost two-thirds had less than 50 employees.

Although the Chinese design organizations tend to be small, the distribution of firm sizes is, however, somewhat less tilted towards very small firms than in Europe. The largest Chinese firms have about 600 employees, whereas in Europe the largest firm, ARM Ltd, had over 1700 employees in 2007. Using data from the Future Horizons European Fabless Semiconductor Report, which provides data on engineering employee counts of 313 design firms (design houses, fabless and semiconductor IP firms), we can compare the size distributions of Chinese and European design firms. The distributions, as the percentage of firms in different size categories, is shown in Figure 35. The data on Chinese enterprises comes from CCID, with total 491 enterprises.[175]

The size distributions are different. One possible explanation could be that the European ecosystem has evolved for a longer time, leading to a situation where relatively few firms have successfully grown to be dominant players in their segments, either through organic growth or by acquiring smaller firms. In China, the market has expanded very rapidly and competition among firms has been relatively modest until recently. Due to the lower employment costs in China, the number of full time employees is also a less tightly linked with overall productivity and business success than in Europe. iSuppli states that the Chinese semiconductor design industry is polarized with about 50 firms achieving success, and about 500 firms struggling to survive. iSuppli also expects that in the next two years about 100 design enterprises will close down.[176] PwC, in turn, predicts that about 100 core firms will remain competitive.

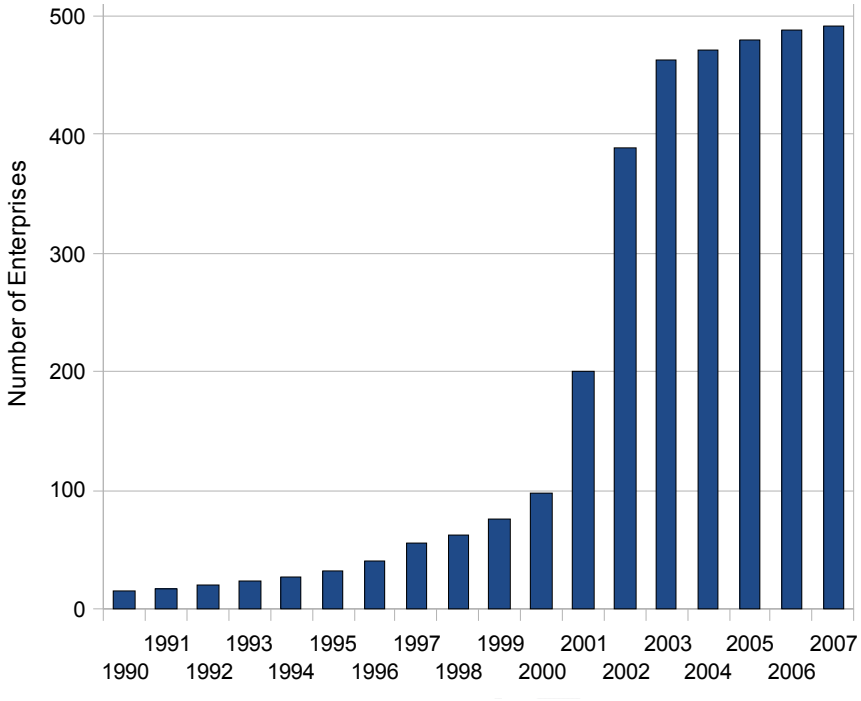
The Chinese IC design enterprises still work with technologies that are several generations behind the leading edge. At present, the top tier of Chinese enterprises design at the 90 nm technology node. Almost 80 percent of the enterprises, however, created designs at over 250 nm geometries in 2007. A relatively complete picture of the Chinese

174 GSA Global Financials Report assigns 257 employees to Actions Semiconductor. This number is also used by PwC, which concludes that Actions was the only Chinese design company that achieved the average sales per employee of the 180 worldwide fabless companies reported by GSA. Actions Semiconductor Investor FAQ, however, reports that the company had 523 full-time employees at the end of 2007.

175 The CCID data include all employees in 2007, whereas Future Horizons only provides data on engineering employees. We use the 2007 Edition of the Future Horizons European Fabless Semiconductor Report, which in some cases gives employee counts that suggest that the data may have been collected in earlier years.

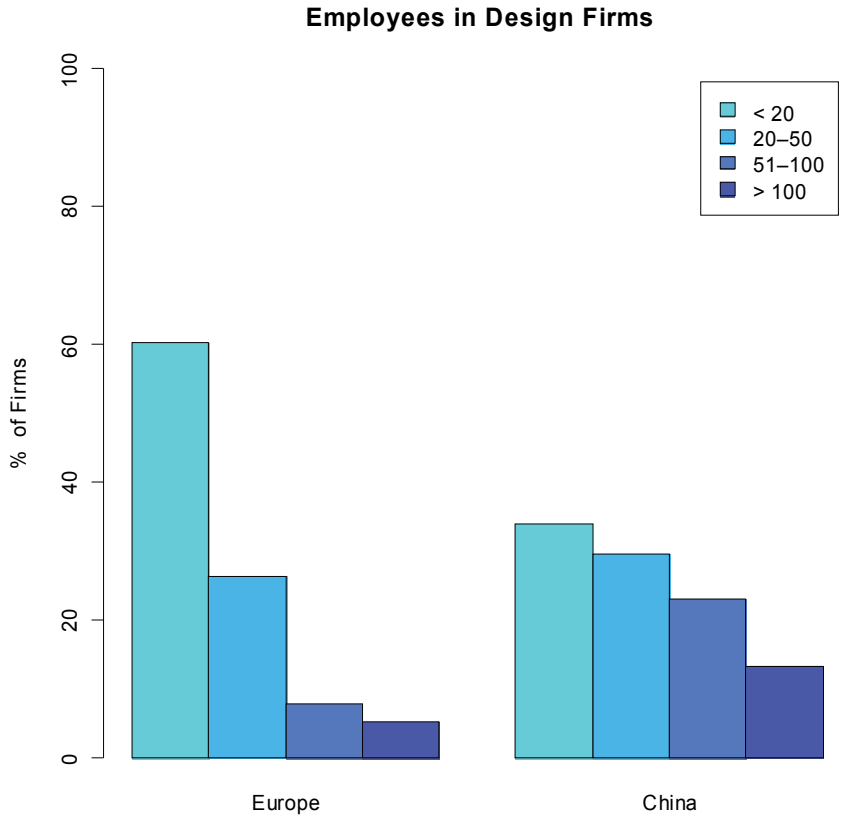
176 McGrath, D. (2008) iSuppli: Setbacks in some China IC firms linger. EE Times Asia, 21 November 2008.

Figure 34: Number of IC design enterprises in China, 1990-2007



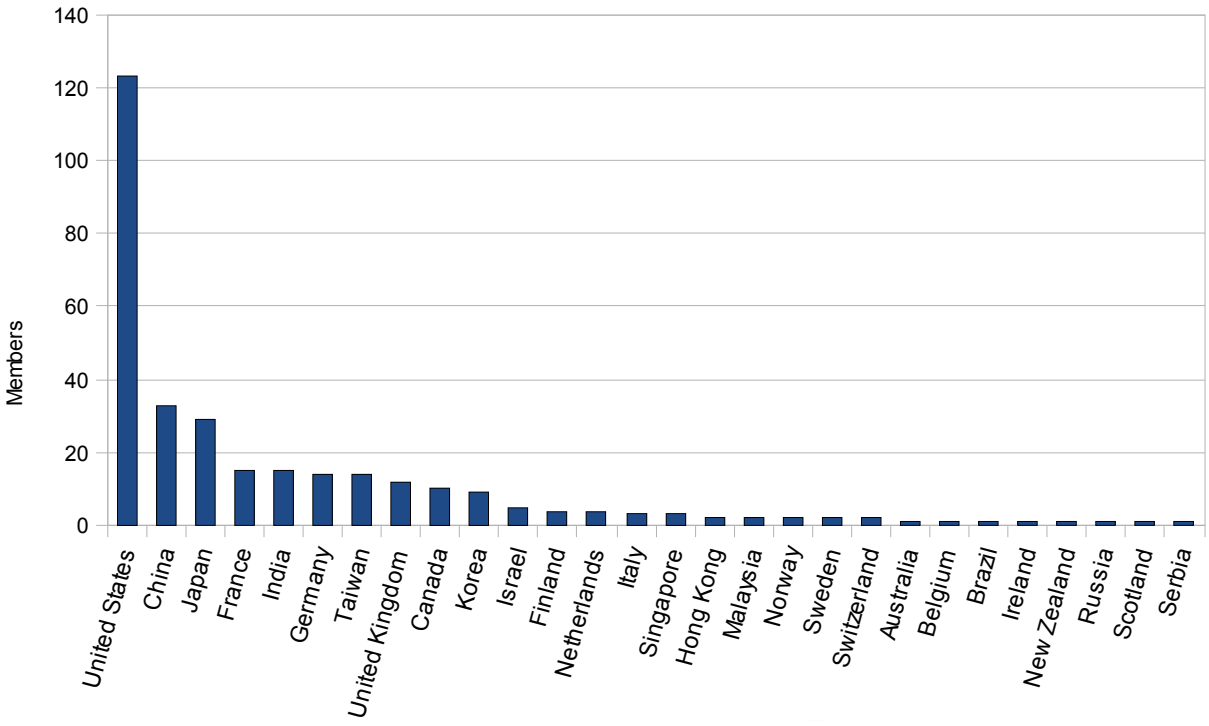
Source: CCID, 2008.

Figure 35: Distribution of enterprise sizes in Chinese and European design firms



Source: Meaning Processing, 2008.

Figure 36: ARM Connected Community members in different countries, 2008



Source: Meaning Processing, 2008.

design firm outputs will be available after the China Semiconductor Industry Association IC Design Branch (CSIA-ICCAD) publishes the first China National IC Procurement manual "China Chip IC Products Collection" in the next months. [177]

Pure-play semiconductor IP vendors are still rare in China, and most of the IP revenues are payments for imported IP. PwC estimates that Chinese semiconductor firms were buying semiconductor IP for about USD 26 million in 2007. This consists mainly of license fees paid by Chinese fabless firms to companies such as ARM and MIPS. Indigenous production of licensable and reusable semiconductor IP is still very limited. We were able to locate 13 firms that marketed semiconductor IP blocks outside China in 2007. These include Shanghai Fullhan Microelectronics, established in 2004, that licenses video coder IP cores; C*Core Technology, which was originally set up to receive the M*Core 32 bit RISC CPU technology from Motorola in 2001; V-Trans Microelectronics, which licenses mixed signal cores for data bus drivers and claims to be able to do analog and mixed signal designs down to 65 nm processes; and Advanced Intellectual Property System Technology (AIPS Microelectronics), which licenses memory and bus controller IP cores.

A somewhat different view on the Chinese design landscape is provided by looking the developer ecosystem of the largest independent IP vendor, ARM Ltd. Chinese companies and research institutes are very actively participating in the ARM Connected Community network. In early 2008, over 10 percent of the 311 ARM Connected Community members had their main address in China and Hong Kong. The number of Chinese partners in the ARM Connected Community was increasing rapidly, with 41 Connected Community members reporting their headquarter address in China and 3 in Hong Kong in November 2008. Only the US

177 CSIA-ICCAD: The Notice to Publish "China Chip IC Products Collection," available at http://www.csia-iccad.net.cn/u/jcdl/iccg/01.html. The deadline for submitting information for the collection was August 30, 2008.

had more members. As noted before, this was partly because also firms that have their main activities outside the US tend to locate their head offices in the US or want to provide a contact address for their US locations. For example, the Chinese fabless firm Spreadtrum lists as its main address its Sunnyvale subsidiary, in California. The number of ARM Connected Community members in different countries in early 2008 is shown in Figure 36, as reported by the Community members.

8.3. Policy Issues

Integrated circuits is listed as one of the key items in information industry development in the 11th Five-Year Plan of China. The core electron devices and high-end general chips are the emphasis areas of the information strategy. The policy aim is to gradually realize a Chinese made core of electron devices, to develop the high-end general chips, to promote industry restructuring, and to enhance Chinese competitiveness.

Linguistic problems make it sometimes difficult to interpret the reality behind political declarations. Considerable policy effort, however, has been dedicated to improve China's semiconductor sector. In recent years, IC design enterprises have been gathered to discuss the importance of "self-innovation" and indigenous innovation as a key success factor.

8.3.1. Export Regulations

Until recently the Wassenaar arrangement[178] on export restrictions for dual-use technologies has substantially limited China's ability to acquire leading-edge products. Both export restrictions and their impact, however, seem to be weakening, at least for the time being. For example, Intel started to build an advanced USD 2.5 billion wafer fabrication facility in Dalian in September 2007, with financial incentives from the Chinese government. This is the first 300mm fab that Intel launches in Asia, and it will cover 163,000 square meters of factory space and host a 15,000 square meter clean room. Intel has declared that the fab will be used to make chipsets, which use process technology that is about two generations behind the leading edge. This fits export regulations that limit the exports to so-called N-2 equipment, or equipment that is two generations behind the most advanced contemporary standard. Intel has already secured a license from the US government to make 90 nm chips in Dalian in 2009. As the Dalian Fab 68 is expected to be in operation in early 2010, it is probable that the fab, in fact, will start the production with 65 nm chips.

In December 2007, IBM announced that it had licensed its next-generation 45nm technology to Semiconductor Manufacturing International Corp. (SMIC), which is the globally third-largest pure-play foundry, based in Shanghai. At present SMIC is shipping wafers at 90 nm process technology, and it expects to deliver chips in 65 nm at the end of 2008. SMIC expects to move to 45 nm processes towards the end of 2009. The process is based on technology licensed from IBM and advanced equipment from ASML Holding NV. SMIC expects to deliver its 32 nm process in the second quarter of 2011, about 18 months behind the technology leaders. Although IBM and SMIC have not discussed their future plans in detail, SMIC has told that it is engaged in talks to license IBM's 32 nm technology.[179]

One reason for the weakened export restrictions is the fact that advanced semiconductor technologies are not controlled by any single

178 The Wassenaar Arrangement on Export Controls for Conventional Arms and Dual-Use Goods and Technologies was established on May 12, 1996. It has 40 participating states, who, at their discretion, restrict exports of dual-use technologies. The current list of restricted products and technologies includes, for example, custom ICs for which either the function or the status of the final equipment is unknown, if the IC is rated to operate above 125 C or – 55 C. The agreement also restricts exports of several wafer fabrication technologies that create features below 180 nm.

179 LaPedus (2008).

country, and restrictions are normally applied only if equivalent equipment is not available from other sources. SMIC has been able to avoid export controls, for example, by buying advanced used equipment from Belgium. According to CCID, already in 2006 2.5 percent of Chinese foundry capacity was for a 90 nm process.

The loosening of Taiwanese export restrictions could also have an important impact in China. The current government in Taiwan has favoured closer ties with mainland China, thus reversing the earlier policy of tight restrictions. Until 2002, Taiwan had a total ban on semiconductor investments in China. Since then, Taiwanese semiconductor firms have gradually started to move to mainland. More recently, firms and policy makers have argued that Taiwan should not be more restrictive in its export policies than, for example, the US. In July 2008, the Taiwanese government abolished the limits on investment in China by companies whose operational headquarters are in Taiwan. Further loosening of export and investment restrictions are expected in 2008 and 2009. As the Taiwanese semiconductor industry had revenues of USD 44.6 billion in 2007, closer ties with Taiwan and the mainland China will potentially have a big impact on the global semiconductor industry. PwC estimates that semiconductor production in Greater China, including Taiwan, Hong Kong and mainland China, represented about 24 percent of the worldwide revenues. In 2007, semiconductor consumption in Greater China represented about 39 percent of the global consumption.

8.3.2. Labour Contract Law

In 2007, China adopted a new Labour Contract Law (LCL), which became effective in January 1, 2008. The new LCL harmonizes regulations that previously have varied across local jurisdictions, and it considerably strengthens employee rights. The law includes sections on probationary periods, redundancy, liquidated damages, severance pay, collective bargaining, noncompete, and part-time employment. Employees who have worked for the employer for ten consecutive years or who have consecutively completed two fixed-term contracts, will have labour contracts without a fixed term. Employers who terminate employees early from a fixed-term contract shall be liable for severance pay. The employee will have the right to terminate the contract with a 30-day advance notice, and immediately if the working conditions are unsafe, or, for example, if the employer fails to pay overtime pay or legally required social insurance. Similarly, the employee may immediately terminate the contract if the employer illegally limits the employee's personal freedom. In such cases, the employer is liable for severance pay.

The new LCL also restricts noncompete clauses in labour contracts to senior managers and senior technicians and other personnel under non-disclosure obligations. If the employer pays for special training, the employer may require a service period, and if the employee terminates the contract before the end of the period, he or she may have to pay back part of the training expense. The LCL also states that when companies plan for lay off more than 20 employees or over 10 percent of total staff, the company needs to provide a 30-day advance notification to the labour union or all employees, consult with either the union or employee representatives, and submit the plans to the labour authorities. The employer is required to retain with priority those employees who have long-term contracts or contracts without fixed term, and employees without other working family members. If the company rehires within six months, the laid-off employees shall be given priority.

According to PwC, the new LCL may substantially increase labour costs and reduce flexibility for many employers. For most multinational companies, the new law will, however, most likely provide a more level playing field as it requires local competitors to provide a level of human resource management practices

that is comparable with those in developed economies. As multinational firms have in recent years typically been required to apply also in China human resource practices that are similar to those in their home countries, the impact of the new law is relatively small for them. Also the main Chinese suppliers to foreign-owned firms and the global market have increasingly been required to meet global standards in human resource management. The potential impact of the new law, therefore, may be to reduce the viability of those Chinese firms that have based their competitiveness on weak employee rights.

A natural consequence of the strengthened labour rights is that labour costs will increase. Chinese firms will therefore have an incentive to move towards higher-value adding activities. A somewhat similar policy was used in Singapore to upgrade its production structure, as was noted before.

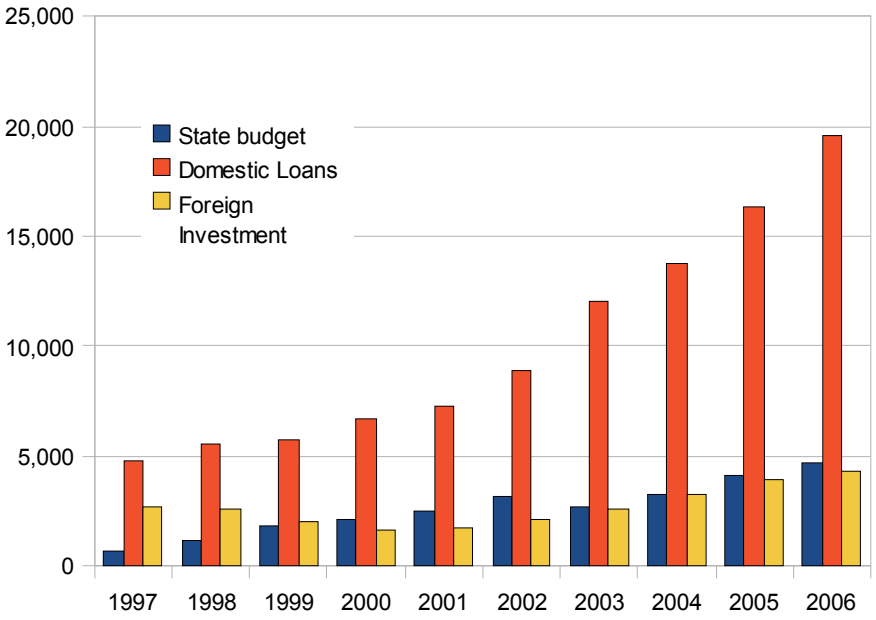
8.3.3. Investment Incentives and the New Corporate Income Tax

The rapid development of the Chinese economy has been based on systematic policies that have aimed at export-oriented growth, industrialization, and the development of national competitiveness. The policies have been inspired by experiences from Japan, and, later, Taiwan and South Korea. On the other hand, since the late 1970s, the Chinese economic policy has also aimed at providing a success model that would show the future for Taiwan and Hong Kong. To an important extent, the policy has been built around Special Economic Zones, which have acted as "experiments" on the new model.

Since 1980, China has established Special Economic Zones in Shenzhen, Zhuhai and Shantou in Guangdong Province and Xiamen in Fujian Province, and designated the entire province of Hainan a special economic zone. The objective was, first, to attract foreign investment, establish industrial investment, and promote export-oriented growth. Later, the objectives were expanded to provide "windows" for new technology, knowledge, management experience, and the new policy of openness. In 1984, China further opened 14 coastal cities –Dalian, Qinhuangdao, Tianjin, Yantai, Qingdao, Lianyungang, Nantong, Shanghai, Ningbo, Wenzhou, Fuzhou, Guangzhou, Zhanjiang and Beihai– to overseas investment. In 1990, the Chinese government decided to open the Pudong New Zone in Shanghai to overseas investment, and opened more cities in the Yangtze River valley. Since 1992, the State Council has opened a number of border cities and, in addition, opened all the capital cities of inland provinces and autonomous regions. In addition, 15 free trade zones, 32 state-level economic and technological development zones, and 53 new- and high-tech industrial development zones have been established in large and medium-sized cities. The five special economic zones aim at integrating science and industry with trade, and they benefit from preferential policies and special managerial systems. The preferential policies include tax holidays, subsidies, and other similar incentives. The most prominent SEZs are now Shenzhen and Pudong.

Combined with low labour costs, these investment and tax incentives have led to extremely rapid expansion of the Chinese economy. For example, one of the early SEZ, Shenzhen, has developed from a small village into a city with a population of over 10 million in 20 years. In the 1980s, the investment was mainly from compatriots in Hong Kong and patriotic overseas Chinese. In the 1990s, also multinational corporations became important investors. In relative terms, foreign investment peaked in 1996, representing almost 12 percent of all investment in China. In absolute terms, both government and foreign investment has continued to grow, however, as can be seen from Figure 37. To a large extent, foreign investment has focused on SEZs.

Figure 37: Total investment in fixed assets in China



Source: National Bureau of Statistics of China, various years.

In 2007, the Chinese government enacted major revisions in its policies on foreign investment and SEZs. The new Corporate Income Tax law (CIT law) replaces the earlier laws that distinguished foreign-owned enterprises (FEs) or foreign-invested enterprises (FIEs) from domestic firms. Although both had a theoretical 33 percent statutory tax rate, FEs and FIEs had a much lower effective tax rate, generally about 15 percent, according to PwC. The new CIT essentially puts domestic and foreign enterprises on a level playing field, imposing a 25 percent tax rate on both. The law aims at simplifying tax regimes, broadening the tax base, lowering tax rates, and strict enforcement.

The new law shifts the focus from foreign investment and export oriented development policy towards knowledge-based indigenous development. The PricewaterhouseCoopers 2008 update on China's impact on the semiconductor industry summarizes the main tax implications of the new CIT law for semiconductor industry as follows:

The tax rate will increase to 25 percent both for domestic and non-domestic firms. For firms in Special Economic Zones that enjoyed a reduced tax rate of 15 percent, the tax rate will gradually increase during the next five years. Existing domestic enterprises and FIEs that have unused tax holidays will be able to use their remaining years of their tax holiday, which, however, has to start in 2008.

High and New Technology Enterprises (HNTE) that meet specific criteria are eligible for a reduced tax rate of 15 percent. The criteria include proprietary intellectual rights, proportion of university graduates employed in R&D, percentage of revenue spent on R&D, and percentage of income from high or new technology products or services. New HNTEs established in SEZs may also be eligible for a two-year tax exemption and a three-year 50 percent tax rate reduction with the holiday commencing from the first profit-generating year. For the first two years, such HNTEs, therefore have a tax rate of zero, increasing to 12.5 percent for the next

three years if the firm makes profit, and further increasing to 15 percent from that on.

In the new CIT law, IC design enterprises are treated in the same way as software enterprises. For example, VAT rebates used for production expansion and R&D will be exempt from CIT. Newly established IC design firms have a two-year tax exemption, followed by a three-year 50 percent tax reduction starting from their first profit-making year. Staff training expenses are tax deductible, and purchase software is allowed to be depreciated or amortized over a minimum period of two years.

IC production companies will be entitled to additional tax preferences, including the shrinking of depreciation periods for production equipment to a minimum of three years and reduced tax rates that depend on the process line-width. For example, IC producers with total investment greater than 8 billion Yuan (about USD 1.1 billion) or which produce ICs with a line-width of less than 250 nm may be eligible for a 15 percent tax rate. From 2008 to 2010, IC firms will also be able to get a 40 percent refund of the taxes they have already paid if they reinvest after-tax profits to increase the registered capital of the firm or a new IC production or assembly enterprise. In the same period, firms that invest after-tax profits in a new IC production or assembly company located in the Western Region may get a 80 percent refund of already paid taxes.

In general, the new CIT law will considerably change the incentives for foreign direct investments and offshoring to China. Many benefits enjoyed by foreigners will disappear, and the incentives will be increasingly uniform across different types of investors. At the same time, the new CIT law concentrates incentives for R&D intensive enterprises and in firms that introduce new advanced technologies, thus improving the Chinese competitiveness in the global marketplace.

8.4. The Five Paths to the Chinese IP Future

Since the early 1990s, Taiwan has become the dominant location for independent foundries. This was based on strong government policies, as well as on tight social networks among expatriates from Taiwan. Today, one out of every four IC products comes from Taiwan. A natural question is: Could China follow the growth path of Taiwan and become a leading producer of key ICT components?

In principle, China could march five alternative paths towards the future. First, the increasing semiconductor manufacturing capabilities could pull increasingly advanced design to China. Second, the large market of semiconductors could pave the way for the Chinese leadership in advanced semiconductor design. Third, government policies could tilt the balance. Fourth, the Chinese innovation system could eventually create competitive advantages that would shift the locus of semiconductor innovation to China. Fifth, the fact that China is currently considerably behind the leading edge could actually become a competitive advantage as the CMOS technology progress slows down, and eventually hits the dead-end. In the following, these alternative routes are briefly discussed.

8.4.1. Manufacturing Pull

Brown and Linden (2009) argue that, to analyze the "manufacturing-pull" hypothesis, we need to differentiate between two primary types of R&D in the chip industry: process development and chip design. In process development, the shift of fabrication to Taiwan (and memory production to South Korea and Taiwan) had, indeed, led to increasing amounts of process R&D in Asia. There are, however, exceptions, an important exception being the equipment suppliers. Process development is actually done jointly by chip manufacturers and equipment manufacturers. The combined R&D spending of equipment

manufacturers is about one quarter that of the chip manufacturers. The leading semiconductor lithography supplier is ASML, headquartered in Veldhoven, the Netherlands. The remaining top ten semiconductor manufacturing equipment suppliers are all based in the US or Japan.

Another exception, according to Brown and Linden, is the growing use of process development alliances. The leading edge fabrication technologies are now developed by large international alliances, such as the Common Platform alliance, built around IBM, Chartered Semiconductor, Samsung, Infineon, Freescale, STMicroelectronics, Toshiba, and others. The Common Platform alliance now includes five of the top ten IC producers, all concentrating their basic process development in IBM's East Fishkill facility in New York.

Although major semiconductor producers, such as Texas Instruments and IBM, are now outsourcing chip fabrication in the future technology generations to either such global alliances or leading independent foundries based in Taiwan, it is becoming increasingly clear that the manufacturing-pull theory does not work in practice.

According to Brown and Linden, the manufacturing-pull effect is even weaker with respect to chip design. Today, the US is still the dominant location for design-based fabless semiconductor firms. Although the US firms are offshoring and outsourcing their activities to Asia, this rarely happens because of fab location. A simple counter example for the manufacturing-pull hypothesis is India, which is the leading offshoring and outsourcing location for IC design. Despite its considerable volume of IC design activities and their rapid growth over the last decade, India still does not have a single semiconductor fabrication facility.

In fact, the old wisdom "fab is the lab" seems to describe best the era of IDMs, in the 1980s. Given the multi-billion dollar investments required for next-generation chip making, and additional multiple billions required for process development, the manufacturing pull hypothesis can be rejected under normal economic conditions. In theory, the Chinese government could, of course, invest such huge amounts of money to set up bleeding-edge facilities that normal economic conditions would not apply. Given the approaching end of CMOS scaling, the investment, however, would probably be difficult to justify also among policymakers.

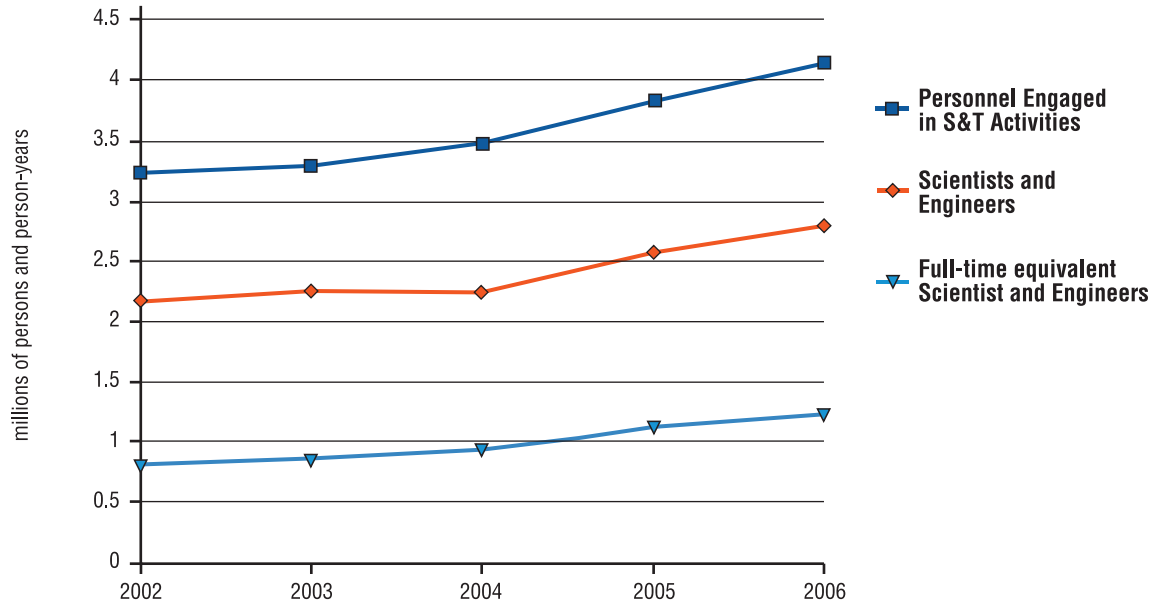
8.4.2. Large-Market Pull

The second path, the "large-market pull," has somewhat more credibility. According to Brown and Linden, a key assumption in this hypothesis is that powerful "national champions" emerge in Asia that eventually will overtake current industry leaders. Given that engineering talent is a critical determinant of the capabilities of a semiconductor company, a key factor is the availability of engineering capabilities.

In fact, the raw numbers are impressive. In year 2006, China had over 12,000 new PhDs in engineering, and over 144,000 new students started their postgraduate studies in engineering. The total enrolment in engineering studies was 412,273 students. In science, the total enrolment was about 135,000. There were 2.8 million scientists and engineers working in science and technology activities in year 2006, according to the National Bureau of Statistics of China. The growth of employment in science and technology is visible in Figure 38, which shows the number of persons engaged in scientific and technical activities.

The number of engineering students in China, however, is only a fraction of the total number of Chinese engineering students. For example, in 2003 there were about 258,000 Chinese students in OECD countries, according to the data from OECD Education database.

Figure 38: Personnel engaged in science and technology activities in China, 2002-2006



Source: National Bureau of Statistics of China,2007.

From 1989 to 2006, Chinese students earned about 45,000 science and engineering doctorates from US universities and institutions. In 2006, citizens of China constituted 26.6 percent of all engineering doctorate recipients and 27.1 percent of all science and engineering doctorates in the US; citizens of India and Korea represented 10.4 percent and 7.4 percent of engineering doctorates, respectively.[180] The growth in the number of doctoral awards granted to Chinese citizens can be seen in Figure 39.

Also a considerable amount of post-doctoral experience is gained outside China. For example, in 2006, almost one third of the new US H-1B temporary work visas for holders of doctorates were granted to persons coming from China. India, in turn, had about 13 percent of H-1B visas, which allow people with special skills and expertise to work as guest workers in the inviting host organization. The distribution of US H-1B visas in the financial year 2006 is shown in Figure 40.[181]

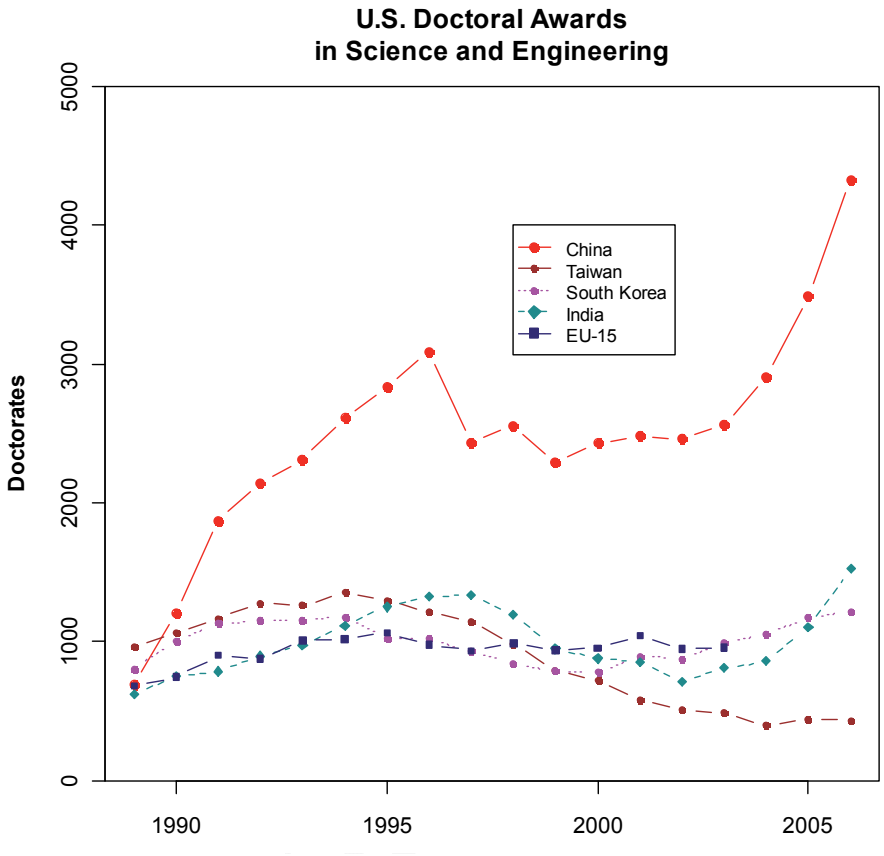
The development of Taiwanese semiconductor industry was to a large extent based on returning expatriates, trained in US universities and leading semiconductor firms. Social networks among ethnic Chinese have also been highly important in setting up the industry in Taiwan.[182] It is therefore clear that China will have considerable potential in shifting the point of gravitation towards mainland China. A critical factor is also the attractiveness of China for returning expatriates. Due to the increasing business opportunities in China and the opening of the economy, many expatriates are now willing to return to China. This is in some contrast with India, for example, where most expatriates state that they want to stay abroad.

180 Falkenheim (2007). In electrical engineering, 77.3 percent of all doctoral awards were granted for non-US citizens.

181 Data from the US Science and Engineering Indicators, 2008.

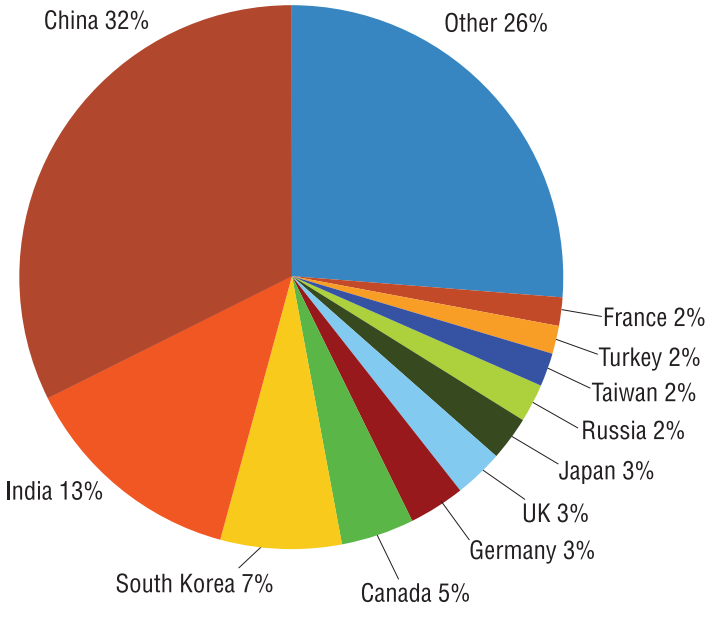
182 Saxenian (1999; 1991). Texas Instruments has been called the "Training Institute" among Taiwanese expats.

Figure 39: PhDs in science and engineering from US institutions for Chinese citizens, 1989-2006



Source: Data from NSF 2006, 2007.

Figure 40: Country of citizenship for new recipients of U.S. H-1B temporary work visas holding doctorates in FY 2006



Source: US Science and Engineering Indicators, 2008.

The development of Taiwan to the leading edge was to some extent slowed by the fact that much of Taiwanese production went to Taiwanese electronic equipment makers, who typically didn't produce technically the most advanced products.[183] To pull the industry to a globally leading position, the producers need to supply the most demanding customers. The development of the Chinese OEM industry, therefore, will have an important role in making or breaking the "large-market pull" hypothesis. If Chinese OEMs, such as Lenovo, Huawei, TCL, ZTE and others will be able to become first-tier vendors in the global market, it is probable that also Chinese semiconductor design firms will follow the suit.

Another factor that could support the large-market pull hypothesis is the fact that product variety and segmentation are important sources of profit. When cultural and local market characteristics are taken into account, products can be customized and made more usable. The Chinese market is culturally and economically quite different from the markets in many developed Western countries, and it therefore makes sense to develop products specifically aimed at the Chinese market. This, indeed, is an important reason for many multinational companies to locate their R&D centres in China. Another important factor has been that, in practice, market access has often required setting up joint ventures and R&D activities in China. Chinese policymakers have followed the model set by Japan, Taiwan, Singapore and Korea, and well understood that long-term economic development requires that China is able to gradually climb the value ladder towards increasingly knowledge-intensive production.

8.4.3. Development Policy

As the histories of the Asian economic tigers show, and now also the Chinese developments confirms, government policy can have a major impact in the development of semiconductor production capabilities. Investment incentives and R&D subsidies have been important in all these countries, and policy-oriented import barriers have been important both in Korea and China. In the case of Korea, import bans were simply used to promote local industry. In the case of China, the large domestic market has also allowed the Chinese authorities to define technology standards that create markets that are relatively protected from global competition. Examples of such standards include the WAPI wireless encryption standard, which was eventually retracted after the US government claimed that the licensing procedure forced disclosure of sensitive information; the third-generation TD-SCDMA mobile standard; and the AVS video compression standard. To a large extent the promotion of such standards is aimed at creating Chinese IPR, to limit the license fees for IPR developed outside China, and to lower product costs, thus leading to increasingly competitive global products.

The Chinese policymakers clearly had played a critical role in the industrial development of China in the last two decades. The current Five Year Plan calls for the development of five IC design companies, each worth 3 billion to 3 billion Yuan, and 10 companies each worth 1 billion to 3 billion Yuan. Although it is improbable that the objectives are met by the end of the current Five Year Plan in 2010, it is clear that the Chinese government believes that IC design is a critical component in the development of Chinese competitiveness. The large-market pull hypothesis, in the context of strong industrial policy, therefore, looks quite viable.

Does this, then, also mean that semiconductor IP activities would move to China in the next years? The conventional answer has been based on labour costs and design capabilities. An apparently simple answer can be found by looking statistical data on costs and educational attainment.

183 See Brown and Linden (2009).

Since the early 1960s, semiconductor firms have offshored their activities to Asia. The driving factor has been low labour costs: in 1985 the hourly compensation of production workers in Hong Kong and Taiwan were about 16 percent of US average hourly earnings of production workers in electronic components and accessories. In Indonesia the hourly compensation was about 4 percent, and in Malaysia about 10 percent of the US earnings.[184] This movement of work, however, was very strongly focused on labour-intensive unskilled tasks. When the first electronics establishment were set up in the territory of Hong Kong in 1961, 71.3 percent of their employees were female. During the rapid growth of the industry in Hong Kong during the 1960s, the share of female workers rose up to 83 percent. Even today, most of the offshoring activities of international semiconductor firms concentrate on packaging, assembly and testing.

In 2004, the average annual salaries for electronics engineers in China were roughly one fourth of those in the US.[185] Part of this difference can probably be explained by the fact that Chinese engineers were less experienced and less productive than their US colleagues. As the salaries of highly educated workers have increased in China, the importance of labour costs is decreasing. Although labour costs obviously have an impact on competitiveness in semiconductor design as the case of India shows, it is also clear that other factors are often more important.

A more useful analysis needs to be based on a model of competence development. Advanced design competence is typically gained by working with advanced design tools and experienced senior designers for highly-demanding customers. A critical question, therefore, is whether there are competence development paths that allow new designers to gain high-level competences.

184 Henderson (1989, 54).
185 Brown and Linden (2009) Ch. 8.

8.4.4. Competence and Innovation System

In principle, the entry barriers in the independent IP vendor business are the same in China as in the other parts of the world. The practical importance of these barriers, however, is different. For example, typically the license costs for high-quality EDA tools cost several hundred thousand dollars per seat, which means that only a small fraction of the average work hour costs are labour costs. The actual fraction is, however, difficult to estimate. As many small Chinese IC design enterprises have been claimed to be engaged in various forms of reverse engineering, it is possible the also EDA software is available at low cost. In any case, the access to advanced EDA tools will be a critical factor in the future development of semiconductor IP industry in China.

Informal competence development routes can also have an important role in generating the required skills. For example, reverse engineering is a relatively demanding technical activity that can develop advanced skills before they can be acquired through formal education and training.

An important source for competitive advantages for the current IP leaders has been their capability to develop vibrant ecosystems that consist of hundreds of firms with complementary products and services. Such ecosystems are difficult to create from scratch and they are also very difficult to copy. The central firms in such ecosystems, therefore, tend to have sustainable competitive advantage.

As technical advances have been very rapid in semiconductor technology, it is possible that technology, in itself, can not create sustainable competitive advantages in the semiconductor IP industry. Rapid technical obsolescence means that, in theory, new entrants could relatively easily introduce new products that have better performance characteristics than the current ones. IP components are, however, by definition, system components. In practice, the competitiveness of

an IP product depends on interrelated products and services that cannot easily be produced by any single actor. Furthermore, and perhaps more importantly, the customers are also part of this ecosystem, with heavy investments in compatible tools and skills. Competition, therefore, occurs in two qualitatively different domains: inside a given ecosystem, among firms that provide competing products and services, and between ecosystems. In both cases, the dominant ecosystem actors are relatively well protected from competition. As Warren East, the CEO of ARM, noted in a recent interview, such an ecosystem can provide a complete solution for customers, thus creating entry barriers for competitors.[186]

The future of Chinese IP business, therefore, depends on the ability of Chinese enterprises to participate in the current and emerging IP ecosystems. Two interesting possibilities arise here: one related to the Chinese innovation model and, another, related to the end of scaling.

As organization researchers have pointed out, the Chinese way of doing business does not fit very well the conventional economic model of markets. Instead of utility-maximizing transactions, business transactions in China are often based on long-term collaboration and trust. For example, the competitiveness of Chinese electronics manufacturers is not so much based on low cost as it is based on the continuous improvement capabilities of Chinese value creation networks. Hagel and Brown, in fact, argue that process networks, such as the one orchestrated by the Hong Kong -based Li & Fung, represent a new type of global ecosystem where development is coordinated across participants.[187] Li & Fung works closely with a network of some 7,500 partner firms. Hagel and Brown contrast this model with traditional business ecosystems that evolved around specific geographic locations such as the Silicon Valley. The key difference, according to Hagel and Brown, is that local business ecosystems focus on advancing specialized practices, whereas process networks focus on organizing the activities across extended business processes.

As Hagel and Brown point out, open process networks can combine effective learning and competence development with efficient production. Potentially, they combine the rapid distributed competence development model that characterizes successful open source software projects with a flexible delivery-focused project model that resembles, for example, high-performance interdisciplinary movie production teams. Open process networks, therefore, could potentially overwhelm traditional organizational forms in domains where innovation and capability development are key sources of competitive advantage. Furthermore, as Castells has noted,[188] the East Asian network-based business systems can also be inherently advantageous when the sociotechnical logic of the informational production paradigm –in other words the network society– converges with the cultural and institutional structures in Asia. As Chinese enterprises are culturally and historically inclined to form networks, and as many key electronics OEMs are now Chinese, loosely coupled and centrally orchestrated process networks could well emerge in the semiconductor industry, allowing Chinese IP vendors to participate in rapid competence development and state-of-the-art innovation processes.

8.4.5. Technical Disruption

The concept of ecosystem is, however, also associated with the concept of extinction. Part of the stability of ecosystems results from their conservative character. Almost by definition, ecosystems evolve gradually and do not sustain revolutions. For example, the success of ARM Connected Community is to an important

186 Shelton (2008).
187 Hagel and Brown (2005).
188 Castells (1996, 173) .

extent based on the fact that the ARM processor architecture is based on a widely used reduced instruction set computing (RISC) model. This model is well understood by software programmers and computer scientists. In fact, the two largest IP vendors, ARM and MIPS, base their products on RISC architectures originally developed in the early 1980s in the parallel research projects in UC Berkeley and Stanford. Could China, for example, develop a radically different ecosystem or orchestrate an efficient process network based on future computing paradigms?

As noted, the end of semiconductor scaling creates interesting opportunities for future IP architectures. In theory, China could leapfrog to new computing paradigms, and establish global leadership in the future IP ecosystems. Although, for example, many small European IP vendors and semiconductor design firms develop advanced computational architectures,[189] it is very difficult to integrate such new computing paradigms within the prevailing mainstream ecosystems. In general, disruptive technologies are best developed in green-field operations.[190] Potentially, China could represent such a "green-field" with relatively little sunken investment and prevailing interests in present generation architectures.

As the end of scaling approaches, the speed of progress in the bleeding-edge slows down. The process of catching up the state-of-the-art, therefore also becomes easier and there is more time for newcomers to learn tools and technologies required to design chips in advanced technologies. As the bleeding-edge becomes increasingly expensive, only few product categories benefit from the most advanced technology, and the majority of designs will be done in older technologies. This means that Chinese designers, who now tend to be two or more generations behind the leading edge, can happily stay one or two generations behind the leading edge. That's where most of the money will be made, anyhow.

Open source software and open source hardware will also potentially transform Chinese capabilities in semiconductor IP. The future semiconductor design market would look quite different if high-quality EDA tools are available in open source. The high cost of proprietary EDA tools, combined with high cost of fabricating custom-designed chips, means that only a relatively small number of new designs are implemented every year. The situation would not immediately change if low-cost or open source EDA tools were available. If, however, new designs could be implemented using low-cost hardware, low cost EDA tools would potentially generate a large variety of new designs. Today, FPGA chips are widely used to produce such low-cost hardware implementations. As the developments in CMOS technology slow down, older-generation technologies start to have longer life-times and their maturation leads to rapidly declining production costs. New designs, therefore, can be implemented for many applications that have not been economically justifiable before. In this process, improved access to sophisticated EDA tools will be an important factor in lowering entry barriers. China would benefit from such developments perhaps more than other regions.

Similarly, access to current leading-edge designs is an important source of learning and competence development. Access barriers have been reduced, for example, by low-cost licenses to universities and also by open source licensing. For example, advanced RISC microprocessor designs are available today through the OpenCores.org, and Sun Microsystems is currently releasing its processor designs through the OpenSPARC.net initiative. Also commercial IP vendors have lowered entry barriers in China. For example, in 2006 ARC International waived its up-front

189 These include various parallel reconfigurable dataflow models for multimedia processing, analog neural hardware, and, for example, self-organizing and transport triggered architectures.

190 See, for example, (Rosenbloom and Christensen 1994; Christensen 1997; Anderson and Tushman 1990; Utterback 1994).

license fees from Chinese fabless firms for designs that are intended for the Chinese market.

In general, design capability is generated by a combination of human, technical, and organizational ingredients. Human capabilities are not something that reside inside humans; instead they are expressed using technical tools that embed accumulated knowledge, and they are implemented by relying on socially and materially distributed knowledge that is mobilized for design tasks. Designs, therefore, are created in complex socio-technical systems, where human knowledge and skill is used in a context of technical tools, and where the results are materialized through social and organizational networks. In the modern connected world, skills and competences are relatively easily acquired if the learner has basic conceptual and theoretical knowledge on which practical competences can be built. In this regard, China is well positioned due to its strong emphasis on general education. The rapidly grown importance of electronics production in China creates many opportunities to use advanced knowledge in computing and semiconductors inside China. There is, therefore, both potential supply and demand of design capabilities in China.

If the entry barriers for semiconductor design are lowered, there is a possibility of a relatively rapid growth of design activities in China. An important condition, however, is that the end demand does not get saturated. The present global IP market shows some signs of saturation, with a small number of dominant firms in the different segments of the industry. The overall industry dynamic, at the end of semiconductor scaling, suggests, however, that the future competition may be based on product variety and the opening up of new innovation segments. If there are no obvious dominant designs, and the long tail of the semiconductor market creates new application areas for design knowledge, the semiconductor design market may experience a phase where saturation is not a problem, and where a large number of alternative product concepts and variations co-exist.

9. Policy Implications

The semiconductor industry is rapidly approaching its most radical technology discontinuity, the end of scaling. Many business models that rely on rapid continuous improvements and price declines in semiconductor technology may fail. Such business models underlie, for example, many of the fastest growing social networking sites on the Internet. This fundamental technical disruption will create interesting new opportunities for new business models, new technologies, and processing architectures. As the technical performance of present-day integrated circuit technologies often surpasses user requirements, and as the creation of bleeding edge chips now cost over € 50 million, a new focus on low-cost processing and configurability is potentially emerging. Instead of chasing the moving boundary of the ultimate physical limits, designers and their customers will ask what is the most reliable and usable solution for a given problem, and what is the optimal and not necessarily most sophisticated technology that can easily address the requirements. As low-cost hardware architectures and implementation platforms become widely available, a new user-centric mode of technology development can rapidly expand the uses and applications of reusable semiconductor IP components.

Almost all future electronic products rely on embedded and interconnected digital and analog designs. An increasing number of these designs are composed from pre-designed virtual components, also known as intellectual property blocks or IP cores. In practice, it is impossible to create complex integrated circuits without such IP cores, and state-of-the-art chips often include several dozens of them. Although a large majority of IP creation activities still occur internally within large firms and are thus invisible in industry statistics, the history of vertical disintegration in the semiconductor industry suggests that also these invisible pools of semiconductor IP can relatively rapidly enter the marketplace. This, in itself, could transform the traditional business logic that underlies the production and development of ICTs.

At the same time, the geographic relocation of the industry continues and new regional hubs emerge. Since the 1970s, Asia has rapidly transformed itself from a developing region into a connected network of leading industrial actors, and the semiconductor industry has played a critical role in this transformation. In a couple of years, China has emerged as the largest consumer of semiconductors worldwide, and a major location for semiconductor production. Europe's future role depends on its capacity to create and grow firms in this knowledge- and research-intensive industry. Although the actual manufacture of integrated circuits is now dominated by the US-based Intel and a small number of Asian firms, Europe has a relatively strong presence in the integrated circuit design segment, and it hosts several leading IP firms.

This, in short, is probably the most exciting time in the history of semiconductors. It is also very exciting for policymakers who try to make sense of semiconductors' future potential.

In reality, many of the major semiconductor firms are international networks. Traditional regional policies have difficulties in interfacing with such actors, and industry statistics often provide data that do not well describe developments that would be relevant for policymakers. In the semiconductor IP business, these problems are somewhat mitigated by the fact that many of the firms are small and located in geographically well-defined places. Yet, even

the smallest actors exist in this industry only because they participate in globally distributed knowledge networks.

As the present study shows, future regional development policies could well be based on creating conditions that facilitate rapid growth in selected hot-spots of large global ecosystems. Policy, therefore, necessarily has to address factors that structure growth dynamics and accelerate innovation, experimentation and absorption of globally generated knowledge. For an individual firm, the key question is which ecosystems it wants to participate and how can it establish itself as a key node in the global network. For policymakers, the question is how the society builds capabilities and processes that allow industrial actors to recognise and appropriate emerging opportunities. This approach puts regional development in a global context and aims to accelerate development in potentially fast-growing niches in a broader ecosystem. Although small niches may represent relatively minor generators of value added in today's economic accounts, they also represent areas of key future competences and domains of above-average economic growth.

New policy approaches are being developed on all continents, and policy can make a difference. The leading industrialised countries in South East Asia became success stories because of their effective and sustained policy interventions. Now they are focusing their policies on the next generation semiconductor-based system technologies, building complete ecosystems that translate and integrate designs into final products. China is still climbing the knowledge-value ladder. The disruptive change generated by the end of semiconductor scaling could well provide a fertile ground for new computing paradigms, and China might well leapfrog into future.

This leaves us with the question: What could Europe do?

9.1. Four Key Trends

According to the present study, several new key trends will shape the future of integrated circuits and semiconductor IP. First, as we approach the end of scaling, it becomes increasingly expensive to waste transistors on a chip. This means that there will be increasing demand for chip designs that are optimised for the problem at hand. Furthermore this means that there will be increasing demand for configurable and reconfigurable hardware architectures. Traditionally, configurability has been achieved by writing application-specific software that runs on general purpose processors. In the future, software will increasingly be used to configure and define hardware. An important side effect is that, when processing architectures can be optimally configured for the problem at hand, also mature low-cost manufacturing technologies can be used to create high-performance chips.

Second, it is increasingly impossible to build advanced chips without pre-designed and pre-tested sub-components. Chip design is increasingly about mixing, matching and modifying existing IP cores. The level of design abstraction is therefore now rising from bits to behaviour. Yet, the lack of sophisticated system development tools and standardised component interfaces currently slows down this move to system-level design.

Third, the dynamics and mindsets in the semiconductor industry are changing. For the last four decades, both the IC industry and the broader ICT industry have been driven by the assumption that the cost of computing and communication declines rapidly. In the future, this assumption does not work anymore. New sources of innovation become important for value creation, and new actors become networked in the technology and product creation process.

Fourth, semiconductor user industries are also increasingly being driven by new open and

distributed innovation models. As information processing products become embedded in our material environment and bundled with services over the product life-time, processing components need to be reconfigurable. When the underlying hardware architectures become reconfigurable, user-centric innovation modes become possible also in semiconductor hardware. This opens up new growth paths for future ICTs.

9.2. Policy Alternatives

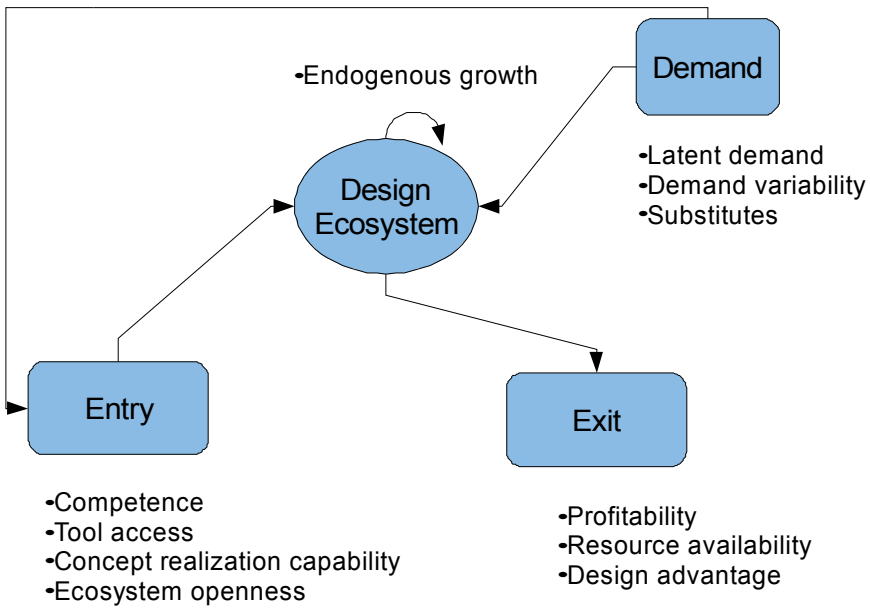
One way to realise the growth potential in semiconductor design is to lower barriers for new entrants. Figure 41 lists some key entry barriers where policy could make a difference. We discuss examples of these below.

9.2.1. Competence Development

For new entrants, participation in the design ecosystem requires skills and competences that are relatively scarce. As the cost of advanced designs is measured in millions of dollars, competence development opportunities are rare, and now increasingly focus on FPGA designs. Although formal education can produce some of the required skills, the declining number of new design projects and the resulting decline in the demand for skilled designers makes skill acquisition in this domain relatively unattractive for potential designers. There are few possibilities to play around and experiment with designs and their modifications, resulting in slow competence development and reduced innovation capacity in the domain. A capability-oriented policy could aim to create new opportunities to experiment and explore technologies and tools that support competence development. This could turn the industry to a new growth path. Two examples are given below.

Important informal learning processes occur in communities of practice, where novices can both observe more skilled actors and participate with the support of peers. Open source software communities are prime examples of such open

Figure 41: Dynamics of the IP design ecosystem



Source: Meaning Processing.

communities of practice. Policies that support development of open innovation ecosystems can therefore be important tools to facilitate both entry and the endogenous growth of the system. Open ecosystem policies need to address openness on technical, social, and cognitive levels. Today, we do not have sufficiently well-developed models for ecosystem evolution. Improved models could therefore be useful for policy support.

As the history of computing shows, advanced capabilities and skills are often created outside the formal educational system. The microcomputer revolution was to a large extent created by hobbyists, and many video, audio and general purpose processor IP firms have their roots in hobbyist computer game and demo programming. Policies that pave the way for enthusiastic experimenters and hobbyists could potentially be highly influential in generating new skilled designers and new innovative applications of technology. Industry-focused policies could therefore be complemented by competence development policies aimed at non-commercial actors.

9.2.2. Expanded Access to Design Tools

In ICT, the economics of software and hardware are different partly because the creation of commercially interesting hardware has required considerable investment and access to leading edge technologies and tools. It is possible to write a demonstration version of a new software system at a very low cost, whereas new hardware often requires several million dollars as front-end investment. The entry cost is high partly because state-of-the-art Electronic Design Automation (EDA) tools are expensive. Although the leading design tool vendors license their tools to educational institutions at a small fraction of the cost of their commercial licences –typically measured in hundreds of thousands of dollars– the use of these tools really makes sense only when the designs are actually implemented. Access to educational licences also requires enrolment in university courses where the tools are used.

One may compare the situation with software development, where compilers and other tools are widely available at low and no cost. Although the complexity of hardware design software is not fundamentally greater than, for example, modern program compilers or operating systems, the EDA market is now structured around a small number of customers. This market structure originates in the era where the current EDA vendors were spun off from major integrated device manufacturers, and it is supported by the fact that the implementation of designs requires heavy front-end investments and large customers. Broad access to design tools would facilitate both competence development and innovation. Components of the design tool chain could be developed, for example, in EU research projects that build open tool infrastructure for future processing architectures. Open source tool chains and design platforms could warrant policy support, research, and development. Policymakers could also benefit from a study that highlights the characteristics of alternative business models that can be built on open design tool infrastructures.

9.2.3. Low-Cost Design Realisation Capabilities

One way to address the entry challenge would be to create low-cost implementation paths that rely on, for example, mature chip manufacture technologies and new design and implementation approaches that make these older technologies useful. Figuratively, this approach would amount to “rising the tail of the long tail.” Although the most advanced and complex designs will also require leading-edge chip technologies in the future, the height of the first entry step is the critical factor for new entrants. When new designs can be realised at low cost, many new designs become viable.

Low-cost realisation paths could be created also by sharing chip manufacturing costs and by using new realisation technologies. This approach is now becoming popular in several Asian countries. For example, Hong Kong Science &

Technology Parks (HKSTP) recently signed a collaboration agreement with the Japanese e-Shuttle to provide silicon shuttle services for start-up integrated circuit design houses in Asia. e-Shuttle, a subsidiary of Fujitsu, provides electron beam direct writing technology at low cost to small and medium-sized firms. HKSTP, in turn, will provide development support and remote access to design tools. European policymakers could benefit from a study that evaluates alternatives for setting similar facilities for European designers.

The high manufacturing costs can also be avoided by using configurable chips that provide flexible platforms for designs. FPGAs are now widely used for this purpose; new approaches, such as software defined silicon and general purpose reconfigurable architectures, could also open the design space for new innovations. At some point, radical new implementation technologies, such as printed electronics, could become viable solutions in some domains. A future-oriented study on alternative low-cost implementation technologies could support policymaking in this area.

System-level design tools that explicitly address reusability and provide open interfaces are also important in enabling modular IP development and low-cost integration. Industry efforts, such as the US-based Open Core Protocol International Partnership (OCP-IP), exist in this domain. These efforts could be complemented by broader initiatives that, for example, consider the impact of the end of scaling and new processing architectures. This could be supported on research that focuses on future system-level design tool architectures and interfaces.

9.2.4. New Design Advantages

The end of scaling will create a demand for new processing architectures. Almost by definition, the new architectures implement new disruptive paradigms. They therefore tend to be peripheral in the current academic and industrial context. The potential importance of such new paradigms suggests that search and development of new computational paradigms and their physical implementations could be strongly supported.

It is important to realise that many current processing architectures are built using abstractions that are difficult or impossible to link with the physical world. This is becoming increasingly visible as processing is embedded in almost all products and environments. For several decades, the continuing success of semiconductor scaling and the resulting improvements in processing power have made it unattractive to rethink conventional processing architectures. In the future, new computational models that, for example, combine analogue and digital processing and build on various reconfigurable data flow architectures, could become increasingly important. A systematic mapping of existing and emerging computational paradigms would help policymakers in locating research gaps and opportunities.

9.2.5. Characterisation of Latent Demand and Supply Through Roadmap Activities

Although, for example, the EU ARTEMIS Joint Technology Initiative could provide opportunities for developing the European semiconductor IP architectures, it is important to note that a large majority of the current IP vendors are very small. Their interests are not necessarily highly visible in policy initiatives that are driven by the interests of major industrial actors. The small size of many existing IP vendors and new entrants also makes it difficult for them to join the EU research programmes. It could, therefore, be useful to create a relatively strongly policy-oriented platform where small IP firms could engage with low effort and good cost-benefit ratio in defining road maps for the industry that is approaching a major disruption. For example, the current study could be used as a starting point for a project that

aims at broad participation of semiconductor IP and design enterprises, resulting in a bottom-up road map and scenarios for the future of IP architectures, interoperability standards and design tool development.

9.2.6. Intellectual Property Legislation

Although intellectual property rights legislation and enforcement are obviously an issue in the semiconductor IP industry, the present study has mainly skipped the topic. For example, it is estimated that a large fraction of the small Chinese semiconductor design firms are engaged in various forms of reverse engineering and some observers claim that up to two-thirds of EDA tools in China are illegal copies. The semiconductor design industry, as well as major integrated device manufactures are, therefore, actively addressing technical, cultural and political challenges that would reduce the production of counterfeit integrated circuits and unlicensed copying.

It is important to note that stronger IPR legislation and increased control of rights holders in the IP industry do not necessarily or automatically lead to a stronger semiconductor IP industry. Vendors with different business models have different requirements for IPR legislation and its enforcement. As the question of the optimal IPR regimes greatly exceeds the scope of semiconductor IP, we simply noted above that the linkages between innovation and IPR are complex, actively debated, and not well understood today. As the IPR structure greatly influences innovation dynamics and ecosystem development, a specific study on the impact of IPR in semiconductor IP ecosystems would be useful for future policymaking.

9.2.7. Ecosystem Openness and New Innovation Models

A potentially important research question that emerged during the present study is the viability of open source hardware projects. There are now many hardware IP architectures available in open source form and, for example, Sun Microsystems is currently releasing its advanced SPARC processor designs as open source. The availability of high-quality architectures in open source could change the current IP vendor landscape. More importantly, if the distributed collaborative open source innovation model would work in the integrated circuit hardware domain, the historical growth dynamics in hardware design could change considerably. Until today, this possibility has not been explored except briefly during the present study. It appears that –although the open source software development model often seems to fail in hardware domains– with suitable modifications and support processes open innovation models could also become effective in IP architecture development. A better understanding of these conditions could support faster growth of ecosystems that develop semiconductor IP processing architectures, and lead to new policy instruments.

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11. Appendix: The IC Design Process

To understand the value creation alternatives in the semiconductor IP business, it is necessary to understand the steps that are needed to create designs. The activities differ somewhat depending on the type of design. For example, designs that include analog components, such as wireless interfaces and sensors, typically require modelling the physical characteristics of the component. Purely logic devices, such as microprocessors and microcontrollers, in contrast, are created in a design process that focuses on describing the behavioural characteristics of the chip.

Two main design flows exist: one that is used to create application specific integrated circuits (ASICs) and one that is used with field-programmable gate arrays (FPGAs).

In ASIC design, logic and other electronic circuitry is converted from high-level functional description to a physical layout that is transferred on silicon wafers in a complex process that builds and interconnects microscopic components to a functional design. Typically, a single wafer is used to make a large number of identical chips, or die, which are subsequently cut and packaged as an integrated circuits.

Field Programmable Gate Arrays (FPGAs), in contrast, are fully standardized chips, which, however, can be configured after manufacturing. The early FPGAs could only be programmed once, essentially by burning fuses or by creating "short-circuits" on a chip so that a specific logic architecture emerged. Modern FPGAs, however, are fully programmable and can also be reconfigured remotely, for example, through the Internet. Modern FPGA chips also often contain embedded ASIC blocks for memory and signal processing. Currently, the two largest providers of FPGA chips are Xilinx and Altera, which together share about 80 percent of the FPGA market.

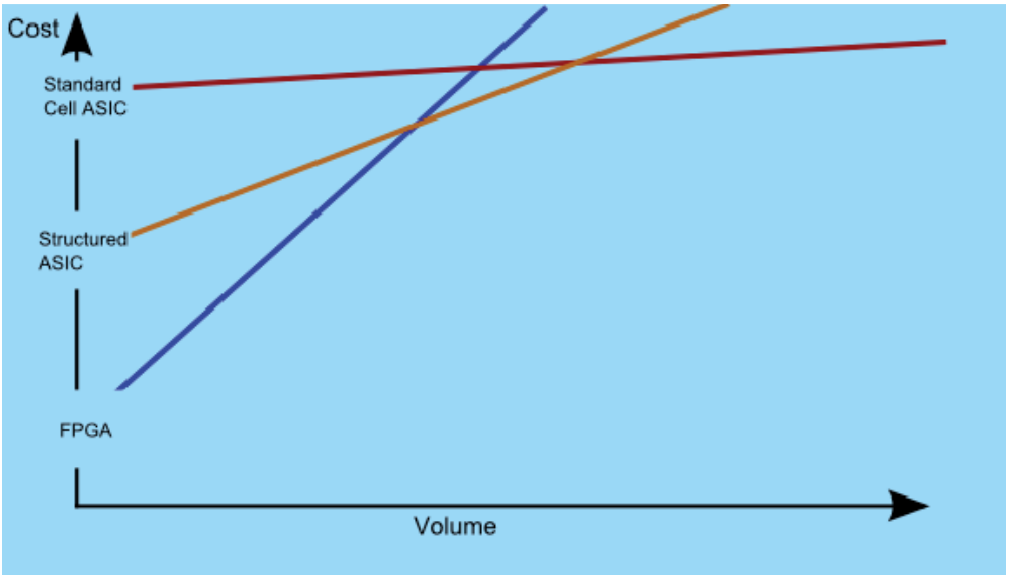
When the first FPGAs were introduced by Xilinx in the 1980s, the number of transistors on a chip were limited, and only relatively simple functions could be implemented using FPGAs. The rapid scaling of chip features, however, means that today it is possible to download several microprocessors and complete digital systems onto a FPGA. As FPGAs consist of many configurable logic blocks they are also inherently parallel in their architecture. FPGAs are, therefore, increasingly being used for high-performance computing.

IP cores can be, and often are, implemented on both technologies. Many IP cores are first developed and implemented using a FPGA. If the customer product is manufactured in large volumes, the design is converted into a custom-made ASIC.

These main routes to customer-specific chips have very different characteristics and trade-offs. The main difference is that front-end costs of ASICs can be very large, measured in tens of millions of USD, whereas commercial FPGA chips and development platforms can cost only tens of dollars.[191] Errors in the ASIC design can become extremely expensive, as new mask sets may need to be created and the manufacturing process often has to be started anew. Moreover, design errors that are discovered after the chip is manufactured, can lead to a new manufacturing cycle that may take several months. Specifically in consumer electronics, where time to market is

191 The up-front costs of leading-edge ASIC are today $40 or $50 million and a completed device may cost today up to 100 million USD.

Figure 42: Cost curves for different IC technologies



a critical factor in profitability, such a delay can kill a product. According to industry experts, at present, over 50 percent of ASIC designs require such re-spins. In bleeding-edge ASIC technologies, the risk of errors increases.

The main benefit of ASICs is that, after the non-recurring costs are paid, the marginal cost of producing new copies of the chip are low. Custom-developed ASICs can also be optimized for the design in question, which can be highly important when, for example, chip size and power consumption are important.

A traditional ASIC uses a cell-based design, where logic gates and other components are created by depositing semiconductor substrates and metal and isolation layers on top of each other. Leading-edge ASICs can have several dozens of metal layers. The features on each metal layer are defined by an optical mask that is used to expose the chip. The processing of semiconductor wafers, therefore, may require dozens of exposures through different optical masks, and sophisticated chemical processing that builds the physical features layer by layer. Leading edge chip fabrication technologies can produce feature sizes that are considerably smaller than the wavelength of light used to print the layout.

The high entry costs for fully custom-made ASIC implementations have created an alternative ASIC implementation type, which is based on standardized chips that can be partially configured during manufacturing. These are called structured ASICs. Unlike normal ASICs, where all chip layers are manufactured according to the customer's specifications, most of the metal layers in structured ASICs are fixed, and only a few top layers are left open so that customer logic can be implemented. The cost of manufacturing the basic layers of a structured ASIC chip, therefore, can be amortized across all the customers. This leads to relatively low non-recurring engineering and mask costs. Typically, for a new structured ASIC device they are about 100,000-200,000 USD.

FPGAs typically cost tens of dollars in small volumes, with leading edge products up to several hundred dollars. Compared with the non-recurring engineering costs of even simple ASICs, which can easily be hundreds of thousands of dollars, or more, it is not surprising that FPGAs have emerged as the main entry platform also for ASIC design. Typically, chips and the related software are now developed

XMOS: ASICs without manufacturing

XMOS, founded in 2005 and located in Bristol, UK, is trying to address the ASIC challenge with a new approach that it calls Software Defined Silicon (SDS). XMOS makes a processor chip that consist of several event-driven processors. The processors can be programmed using the high-level C-programming language and processor interconnections can be defined so that the chip architecture can be tailored to specific applications. The architecture also allows chips to be connected to a larger parallel system.

The XMOS SDS chip is based on the parallel Transputer message-passing architecture, originally developed in the 1980s. XMOS was co-founded by David May, Professor of Computer Science at Bristol University and the architect of the Transputer.

"'What if you could start a semiconductor company with $100,000 again?' asks XMOS CEO James Foster.

> 'Our NREs [non-recurring engineering costs] are less than $100,000 and our prototype lead-time is 30 seconds,' according to Foster, 'making $100,000 semiconductor start-ups possible again. Anyone who can program in C, who can get their hands on an XMOS development kit and an XMOS SDS chip, can bring an IC to market.' (Manners, D. "XMOS may make standards unnecessary." Electronics Weekly, 15 July 2008).

XMOS is expected to have its chip in production in the last quarter of 2008. It also intends to bring out a hobbyist kit and robotics design kit at the beginning of 2009, followed by industrial design kit and automotive design kit. The company has stated it targets the $1-$10 price range for its chips.

In June 2008, XMOS won the Intellectual Property and FPGA category of the annual Electron d'or awards. The Electron d'or awards recognise those electronic products the editorial team of Electronique magazine believes have made the biggest impact in the last 12 months. Runners-up in the IP and FPGA category included Actel, Altera and Xilinx.

using FPGA development boards. Products are also often launched using FPGA, which can easily be reprogrammed if bugs are found or if new features are introduced. Only when the product volumes get high, the chip is converted from FPGA to an ASIC chip. The typical cost curves in relation to manufacturing volume are shown in Figure 42.

The leading FPGA vendor Xilinx introduced in 2005 a new low-cost alternative for ASICs. It is based on customer tailored FPGAs. The idea is that after the customer has developed a chip using a standard FPGA, the design can be cost-efficiently manufactured in larger volumes. Most designs use only a fraction of the transistors available on a FPGA chip. After the design is ready, it is possible to manufacture chips where only the required parts of the chip are tested. This increases the yield of chips and lowers the cost. According to Xilinx, the non-recurring and mask costs for such customer FPGAs can be as low as 75,000 USD, and their unit costs are lower than for structured ASICs.

One new semiconductor start-up that tries to solve the challenge of ASIC entry costs is XMOS, based in Bristol, UK. It has developed a processor architecture that can be configured by downloading new software on the chip. XMOS calls its approach Software Defined Silicon. This approach is described in more detail in the box above.

The increasing costs of designing ASICs has led to a rapidly decreasing number of ASIC design starts. Today, the cost of designing a cell-based ASIC can be over 50 million USD. Few firms can afford such costs, and even fewer can afford the risk that the investment does not pay back. In the last four years there has been a 40 percent decline in the design starts for fully customized ASICs.[192]

192 Manners, D. (2008) Semiconductor CEOs have strategy for Asic decline. Electronics Weekly, 13 May 2008.

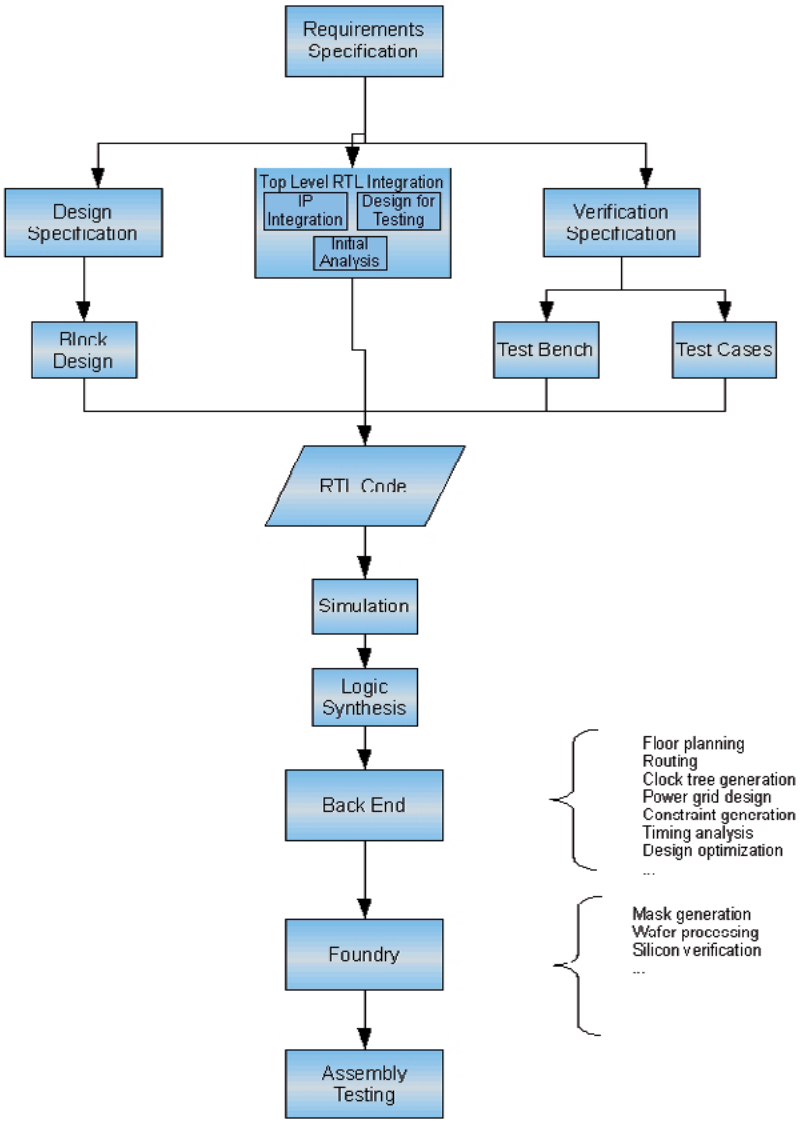
11.1. The ASIC Design Flow

The basic design process for modern system-on-chip ASICs consists of systems design, register transfer level design, logic design, functional verification, physical design, physical verification, and design for manufacturing. A schematic representation of the full ASIC production flow is shown below, in Figure 43.

In *system design*, the designer describes the chip's functions using a high-level language. This phase leads to a high-level behavioural model of the chip.

In *register transfer level (RTL) design*, the flow of data and the transformations that the data undergoes when the chip operates are described. The description is based on hardware description languages (HDLs). The most widely used HDLs are Verilog, based on the C programming language, and VHDL, based on the ADA programming language. RTL is used to describe how data moves between the chip's "registers" that actually store the bits to be processed.

Figure 43: The ASIC production flow



Functional verification checks the RTL or netlist code using automated test benches and simulators to verify that the chip behaves as intended. As the code for complex chips easily contains errors, and as it may be extremely expensive to correct such errors after the chip is produced, verification is a critical design task. The functional verification effort can easily represent 70 or 80 percent of the total work required to design a chip.

In *logic design* or logic "synthesis," the RTL code is converted into a logical diagram of the chip. Logic synthesis generates a data file known as "netlist." The netlist describes the various groups of transistors, or gates, which are implemented on a chip. This conversion or "compiling" of RTL code into a netlist typically uses manufacturing process specific "technology libraries" that describe the physical implementation of basic logic functions. The designer can, for example, optimize the compiled code for space or speed, generating alternative netlists from the same RTL.

In the *physical design* phase the designer uses "place and route" tools to plan the physical location of the transistors and wires connecting them. This phase is also known as "physical synthesis." Typically, the designer first locates the various functional blocks on the available die space, and then determines the locations of gates in each block, and then defines the wiring. As the blocks can consist of millions of transistors, the placement and routing is mainly done automatically, although designers can intervene in this automated process if they consider it necessary. This design phase results in data files that describe the physical structures that need to be manufacturer to create the transistors and interconnections on the chip. This is also know as the "layout view" of the chip. The files normally use the GDS II binary data format. As these binary files can be very large, they used to be written on magnetic tapes that were then sent for manufacturing. This traditional end phase of the design it therefore also know as "tapeout,"

Figure 44: VHDL code for a logic OR circuit

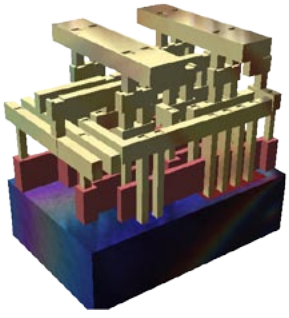
```
entity OR_ent is
port( x: in std_logic;
      y: in std_logic;
      F: out std_logic
);
end OR_ent;

architecture OR_arch of OR_ent is
begin
  process(x, y)
  begin
      if ((x='0') and (y='0')) then
          F <= '0';
      else
          F <= '1';
      end if;
  end process;
end OR_arch;
```

partly because of these magnetic tapes and partly because until 1970's many chip designs were actually manually taped on transparent films.

A physical design also needs to be verified in the *physical verification* phase, as the design must comply with the specific requirements of the manufacturing process that is used to make the chip.

Modern chips also require extensive *design for manufacturing*. The physical design files have to converted into a series of photomasks that are actually used to generate the physical features

Figure 45: Metal layers in a simple logic cell; 3D CAD image



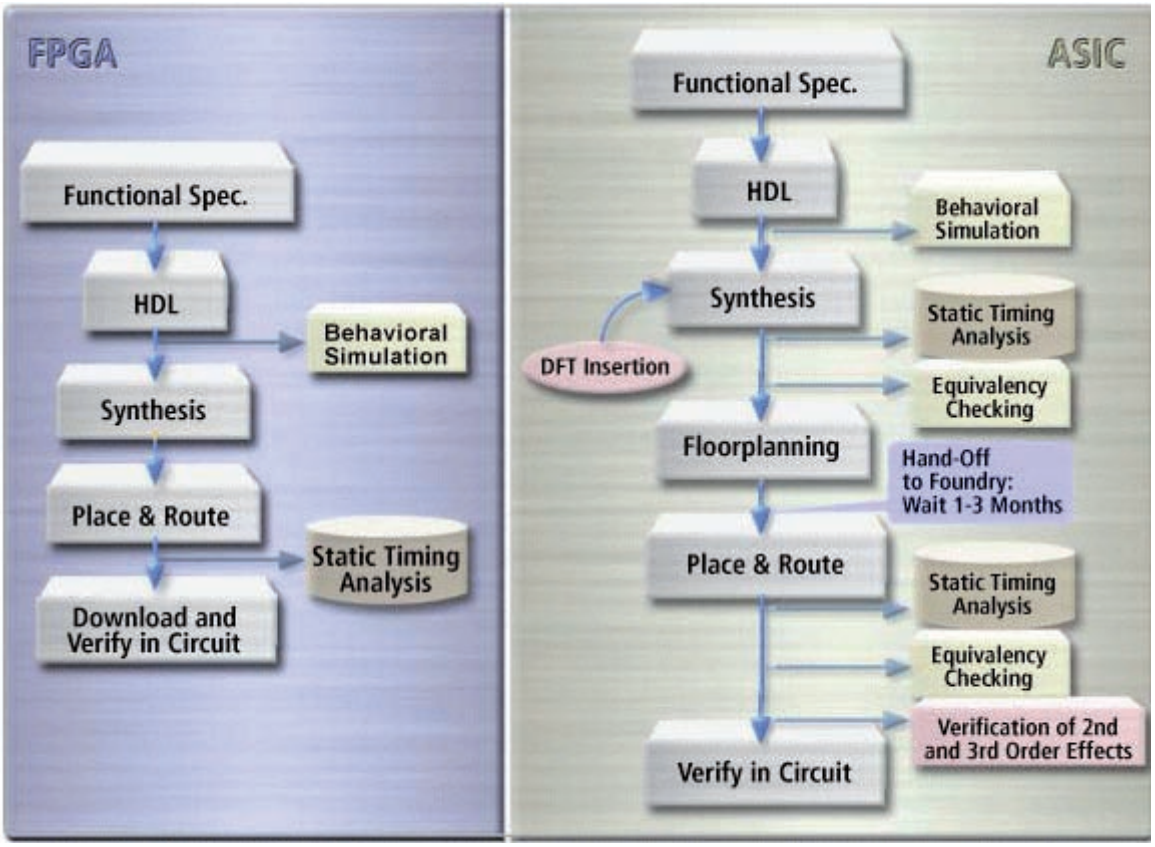
on the different layers of the silicon wafer. As the feature sizes in leading-edge processes are only tens of nanometres, and, for example, smaller than the wavelength used to expose the wafer, it is not possible to simply copy the image of the physical design to the wafer. Instead, the image is distorted and enhanced in multiple ways so that the distortions that occur in the manufacturing process are compensated.

11.2. The FPGA Design Flow

The first phases of the FPGA design flow are basically the same as those for ASICs. System design is followed by RTL level hardware specification. As the hardware in this case consist of an already existing FPGA, the RTL code needs only to be translated so that it can be used to configure the FPGA architecture. After the programming of the FPGA, the system functionality needs to be verified and tested.

The design flows for ASICs and FPGAs are schematically compared in Figure 46.

Figure 46: Production flows for FPGA and ASIC



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Abstract

Semiconductor intellectual property (IP) blocks, also known as IP cores, are reusable design components that are used to build advanced integrated circuits (ICs). It is typically impossible to create new IC designs without pre-designed IP blocks as a starting point. These design components are called 'intellectual property' blocks because they are traded as rights to use and copy the design. Firms that focus on this business model are often called 'chipless' semiconductor firms.

IP cores are perhaps the most knowledge-intensive link in the information economy value chain. They define the capabilities of billions of electronic devices produced every year. As all products are becoming increasingly intelligent and embedded with information processing and communication capabilities, future developments in semiconductor IP will have a profound impact on the future developments in the overall knowledge economy and society.

At present, the IC industry is approaching the most fundamental technological disruption in its history. The rapid incremental innovation that has led to exponential growth in the number of transistors on a chip and expanded the applications of ICT to all areas of human life is about to end. This discontinuity (the end of semiconductor scaling) opens up new business opportunities and shifts the focus of ICT research to new areas.

The main objective of this study is to describe the current state and potential future developments in semiconductor IP, and to relate the outcomes of the study to policy-related discussions relevant to the EU and its Member States.

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